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Rigorous-Simulation-Driven OPC Solution

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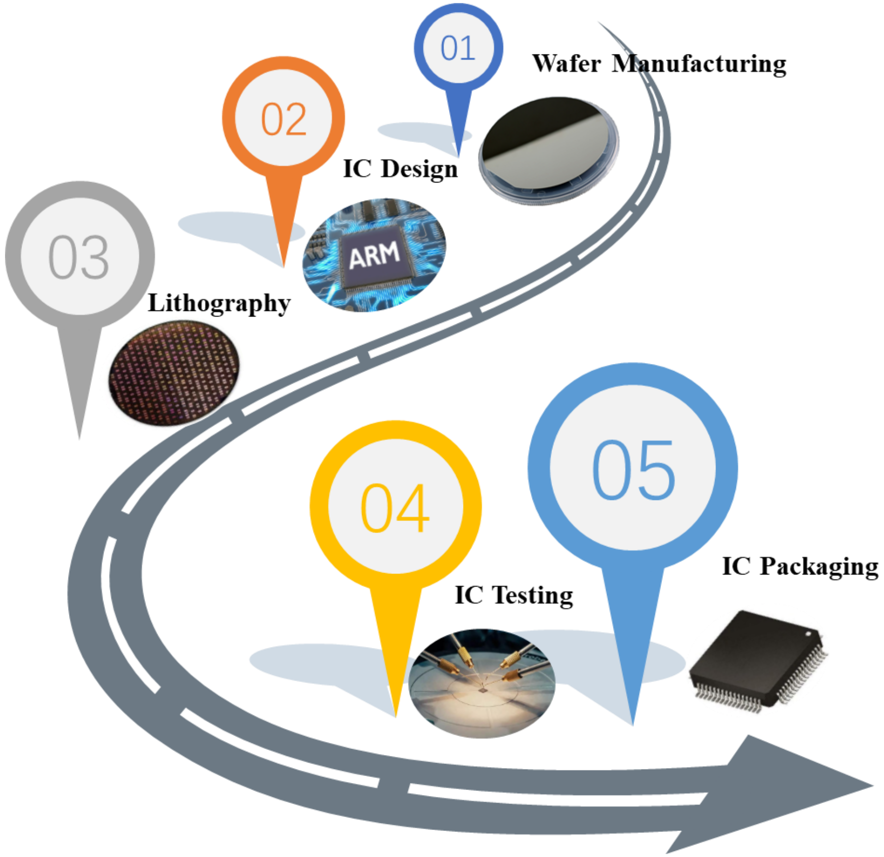
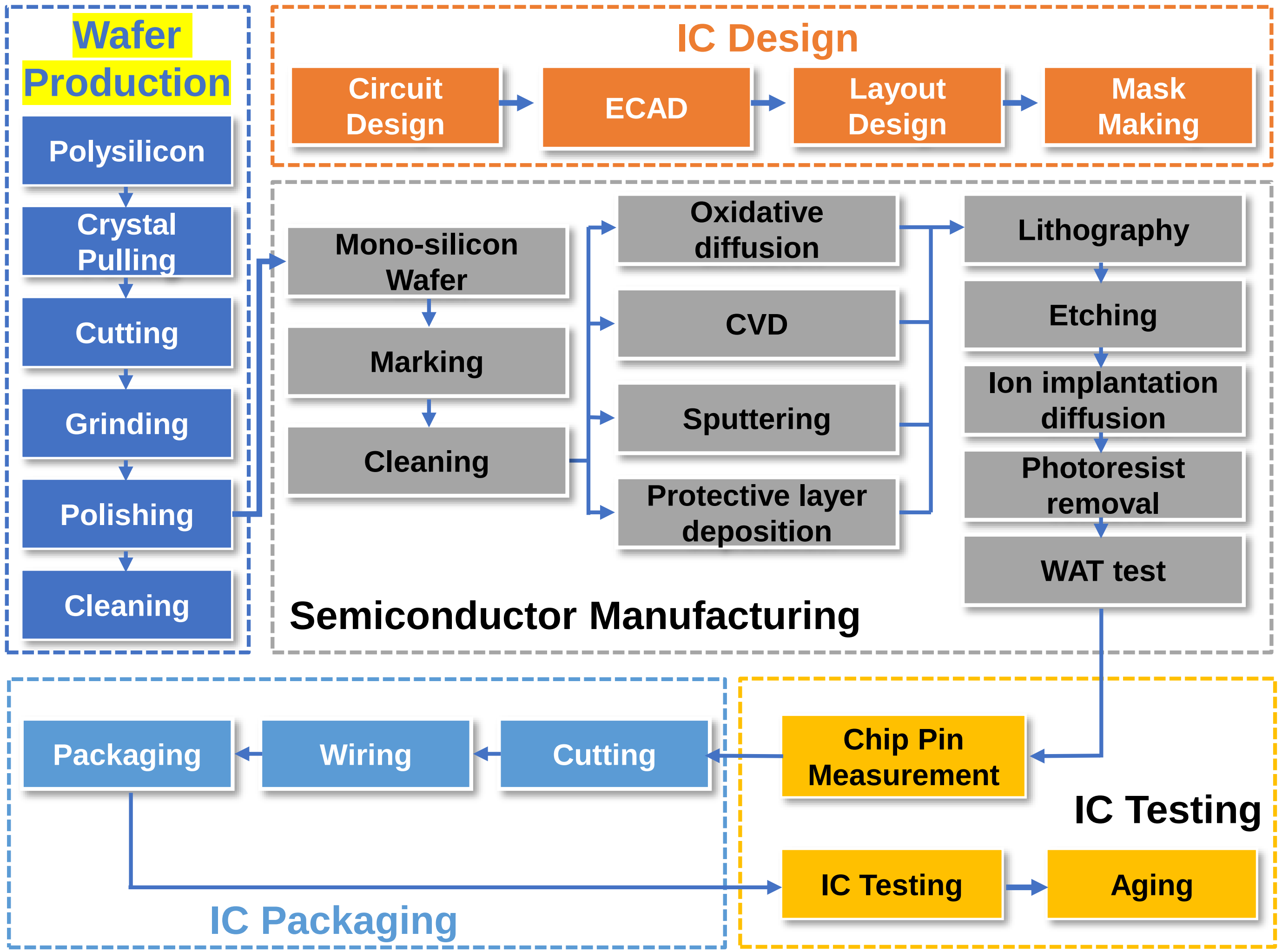
- Background
- Methods
- Examples
- Conclusions

Background - Lithography

Lithography is a key procedure in the manufacturing process of integrated circuits.



Lithography: Time > 50 %, Cost > 1/3



Wafer Production

- Polysilicon
- Crystal Pulling
- Cutting
- Grinding
- Polishing
- Cleaning

IC Design

- Circuit Design
- ECAD
- Layout Design
- Mask Making

Semiconductor Manufacturing

- Mono-silicon Wafer
- Marking
- Cleaning
- Oxidative diffusion
- CVD
- Sputtering
- Protective layer deposition
- Lithography
- Etching
- Ion implantation diffusion
- Photoresist removal
- WAT test

IC Testing

- Chip Pin Measurement
- IC Testing
- Aging

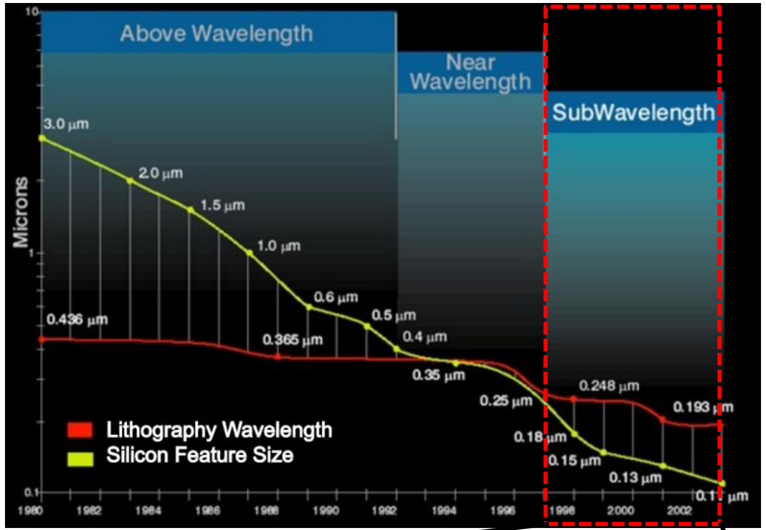
IC Packaging

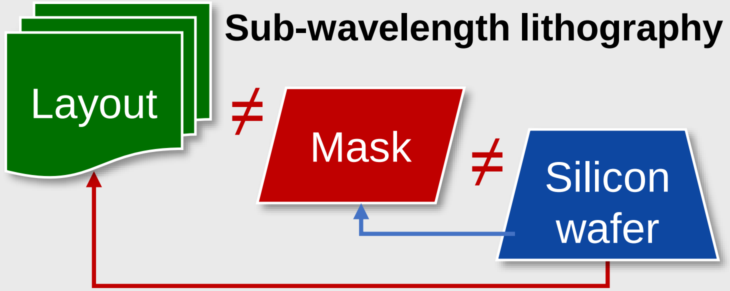
- Cutting
- Wiring
- Packaging

Background – OPE

Lithography process control capability vs. lithography process window

Litho. wavelength vs. silicon feature size

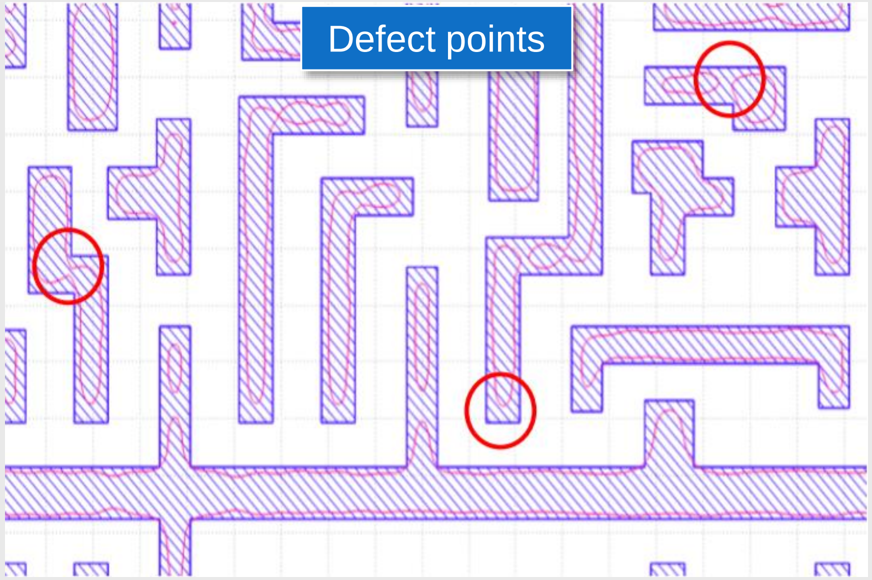




Sub-wavelength lithography

Layout ≠ Mask ≠ Silicon wafer

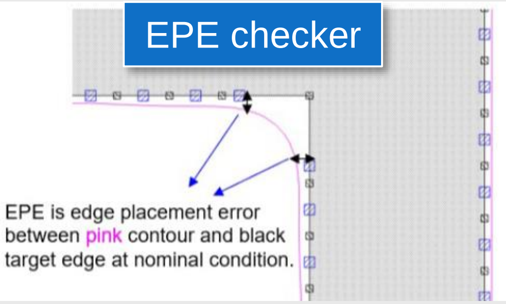
Relationship between layout, mask, and silicon is no longer valid due to process distortion, OPE, and phase shifting.



Defect points

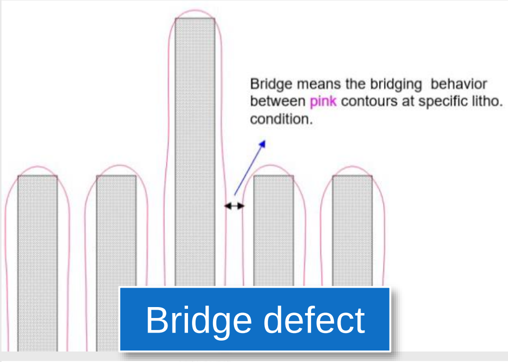
Main performance of OPE:

- Inconsistency between isolated and dense patterns
- Line-end shortening
- Corner rounding



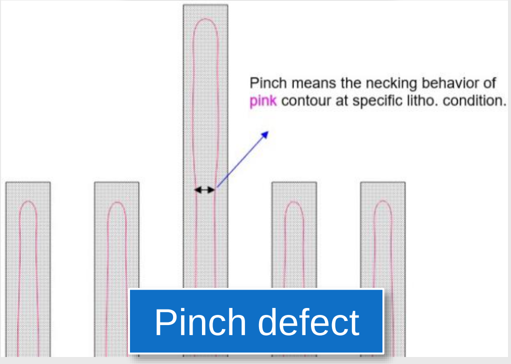
EPE checker

EPE is edge placement error between pink contour and black target edge at nominal condition.



Bridge means the bridging behavior between pink contours at specific litho. condition.

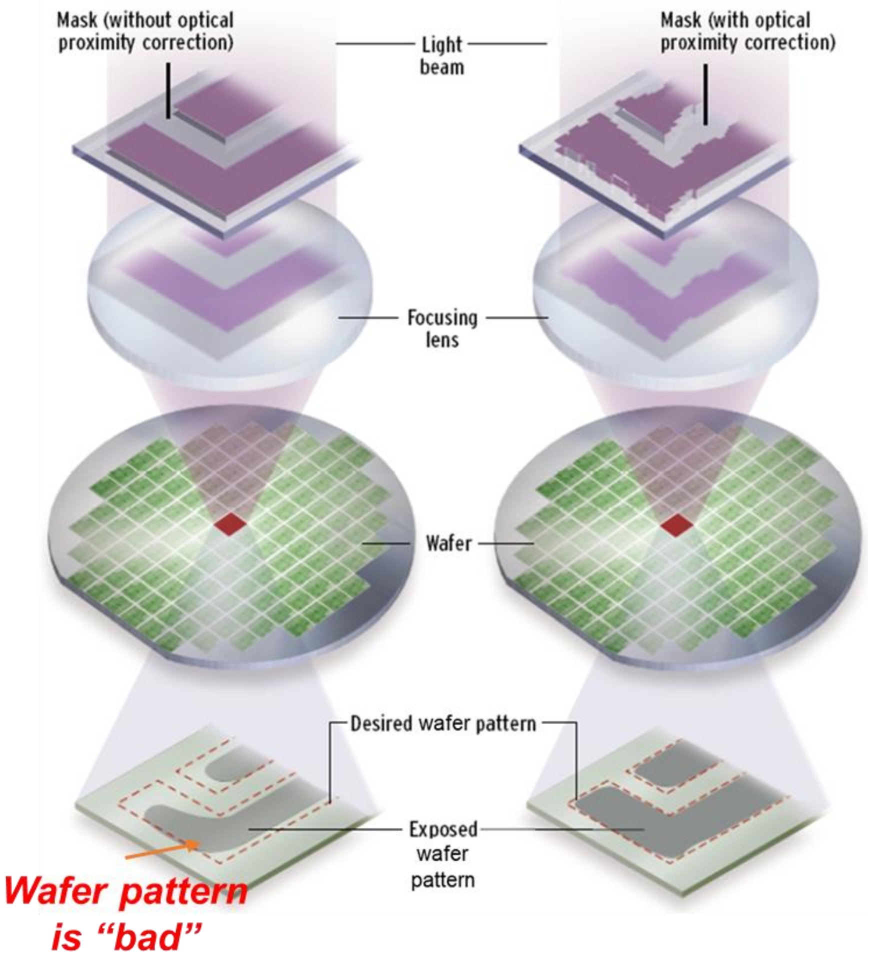
Bridge defect



Pinch means the necking behavior of pink contour at specific litho. condition.

Pinch defect

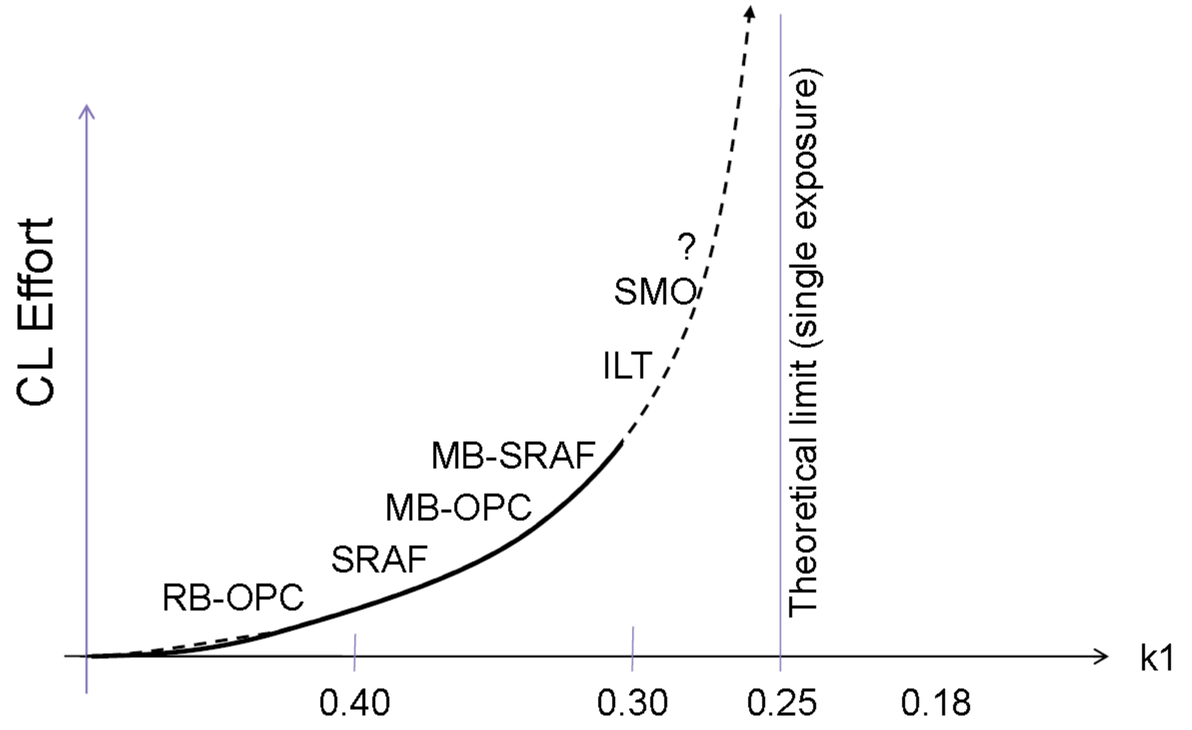
Background - OPC



Computational lithography = k1 scaling

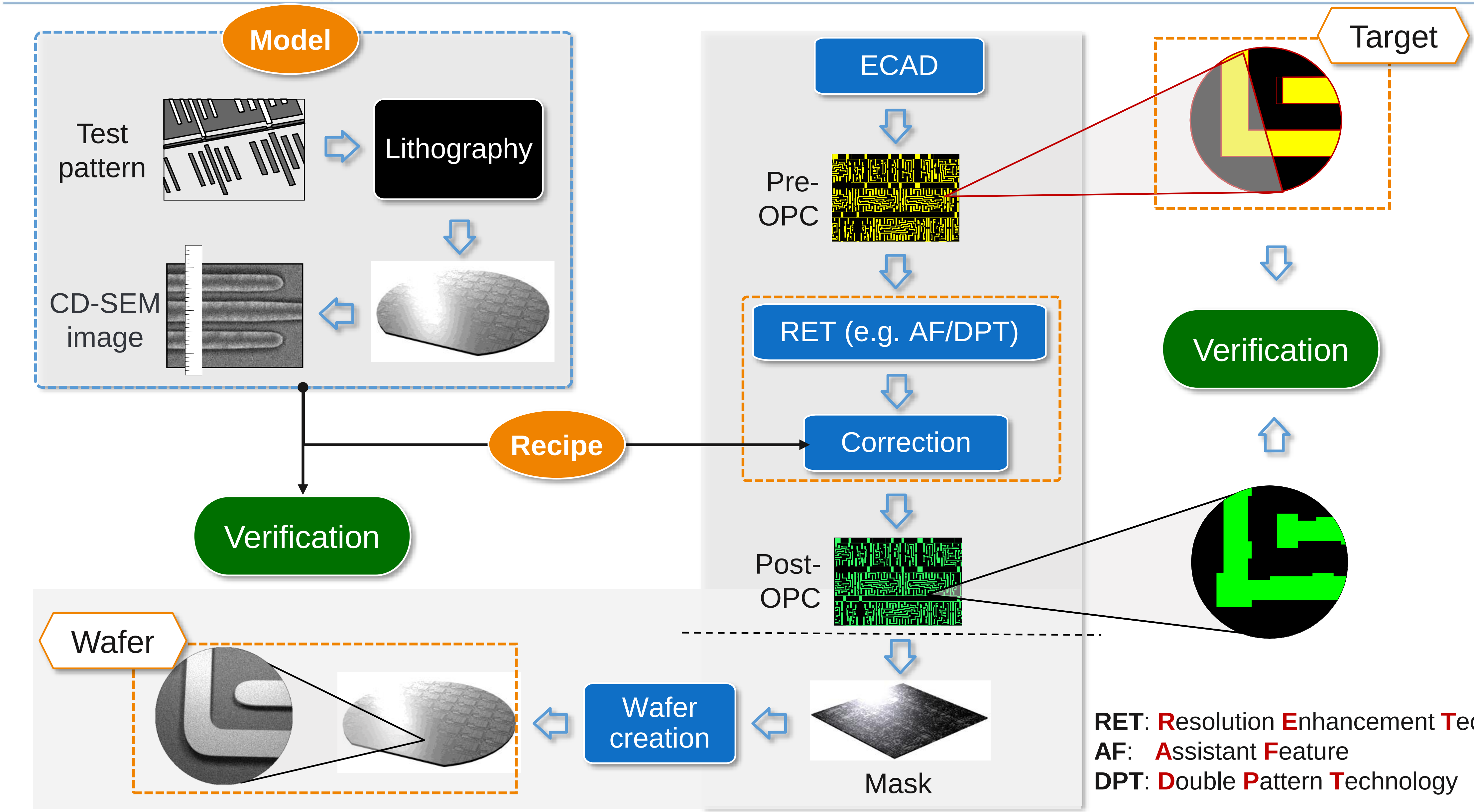
$$CD = k_1 \frac{\lambda}{NA}$$

Focus of CL is to make k1 smaller



- OPC stands for Optical Proximity Correction. It enables low-k1 lithography by changing the pattern shapes on the mask to correct for the non-linear process of printing those patterns on a wafer. The final goal is to improve the device performance and yield.
- The OPC methodology consists of two parts: "Model" and "Recipe".

OPC flow



Model

Test pattern

Lithography

CD-SEM image

Recipe

Verification

ECAD

Pre-OPC

RET (e.g. AF/DPT)

Correction

Post-OPC

Mask

Wafer creation

Wafer

Target

Verification

RET: **R**esolution **E**nhancement **T**echnology
AF: **A**ssistant **F**eature
DPT: **D**ouble **P**attern **T**echnology

Data for OPC solutions

Process parameter

Optic Parameters
- Wavelength, NA
- Source (Sigma or source map)

Film Parameters
- N, K, T for each layer including photoresist

Mask Parameters
- Mask Tone
- Mask Type (PSM or BIN)
- Mask 3D information

Measurement data

Test Graph
- Test Pattern
- Anchor Information (on design rule CD/Space)
- SRAM, StandCell and other design structure
- Hotspot Graphics

Wafer measurement results (corresponding CD and SEM photos)

Correction layout

- GDS file, target graph required by PIE (or provide related bias table)
- Layer mapping

Example of process parameter

Optic parameters

optical settings	example
lambda(nm)	193
NA	1.35
refractive index	1.44
source_type	annular
source parameter	sigma out: 0.9/sigma in: 0.6
source polarization	XY
source map(optional)	XXX.src

Film parameters

film name	n(refraction)	k(extinction)	thickness(nm)
TARC_SOG	1.69	0.24	30
PR	1.74	0.01	250
BARC_SOC	1.53	0.38	130
SiO2	1.46	0	9.6
SiON	2.02	0.55	30
TiN	1.878	1.309	30
Ti	1.234	1.21	20
ESLK	1.57	0.007997	10

Mask parameters

mask info	example
mask tone	clear or dark
mask type	attPSM or altPSM or binary
field transmission and phase	0.06,180

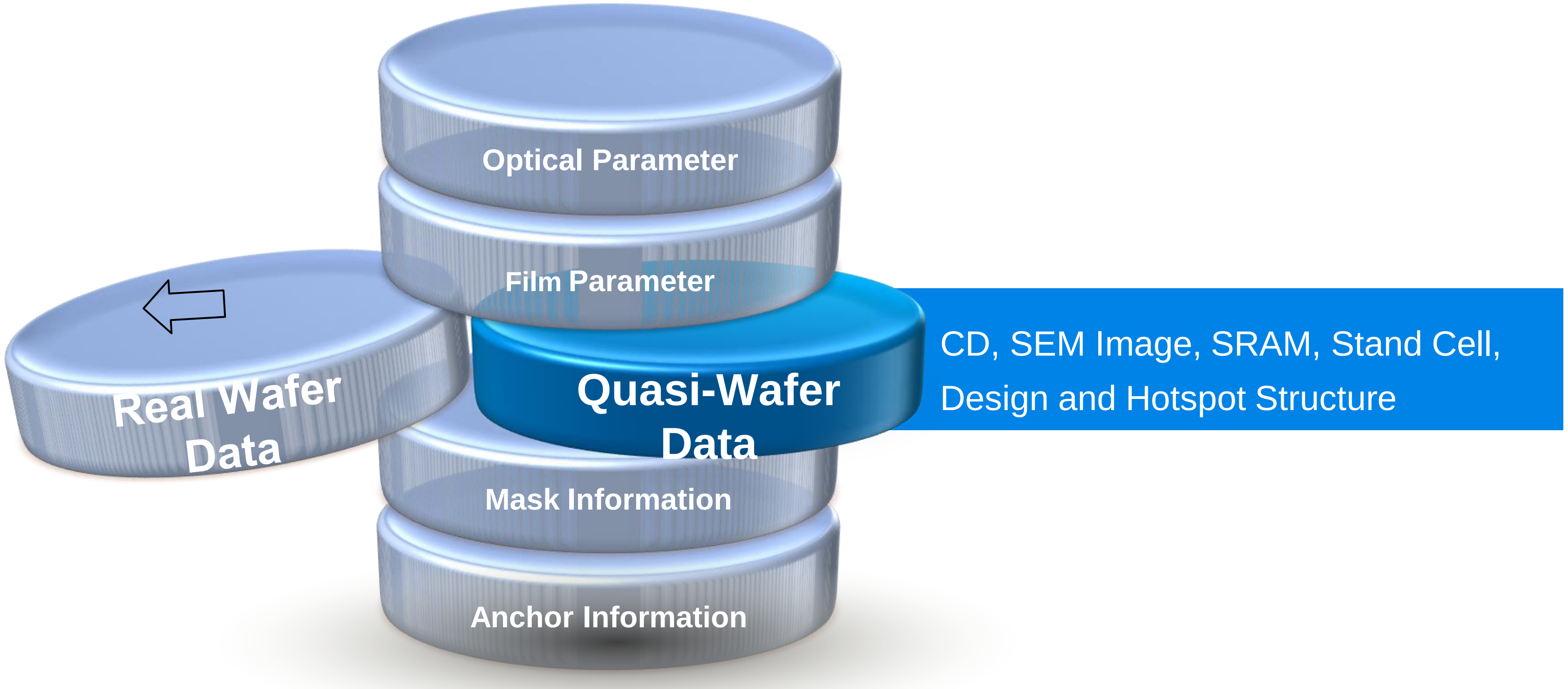
Mask 3D

mask 3D info	example		
mask film stack	n	k	thickness(nm)
substrate(Quarz)	1.56	0	inf
MoSi	2.417	-0.59	68
Substrate etch depth(nm)	10		
Absorber sidewall angle(degree)	87		

In the case of lacking real wafer measurement results, the S-Litho rigorous simulation method can be used to obtain quasi-real data (including simulation of the pattern to be measured, SRAM, standard cell design structures and hotspot simulation SEM results).

Rigorous simulation

Rigorous simulation is a computer-aided simulation technology based on physical and mathematical models of actual production process parameters.



CD, SEM Image, SRAM, Stand Cell, Design and Hotspot Structure

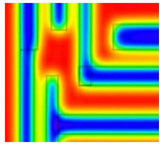
OPC model (quasi-resist model, compact model)

Simulation wafer data replace **real wafer data** in the early stage of process development.

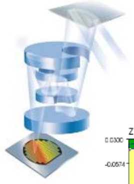
S-Litho

Enabling production-ready solutions by predictive simulation

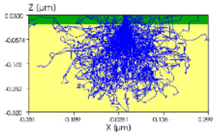
Optical Litho



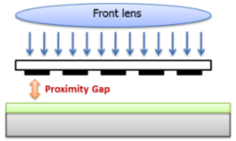
EUV



E-beam



Proximity Printing

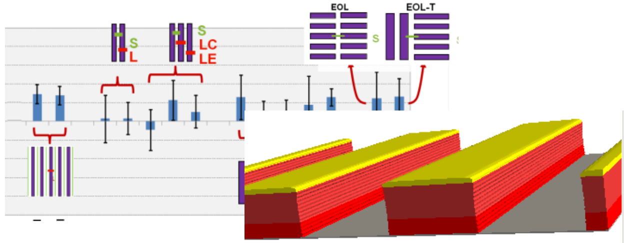


Resist modeling

- Predictive modeling of 3D profiles

Model calibration

- Enable on-site model tuning

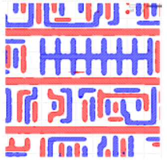


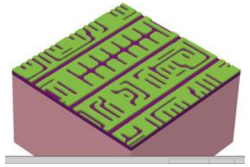
Single simulation environment
for cost effective analysis of technology options

SentaurusLitho

TCAD Interfaces

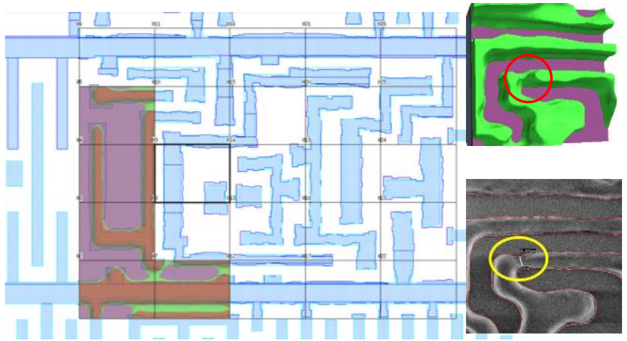
- ➢ Explore interaction between litho, etch, and deposition





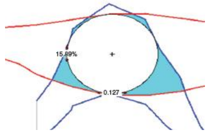
Mask Synthesis Integration

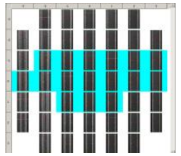
- Layout-centric simulation
- Compact model validation
- Correction and verification



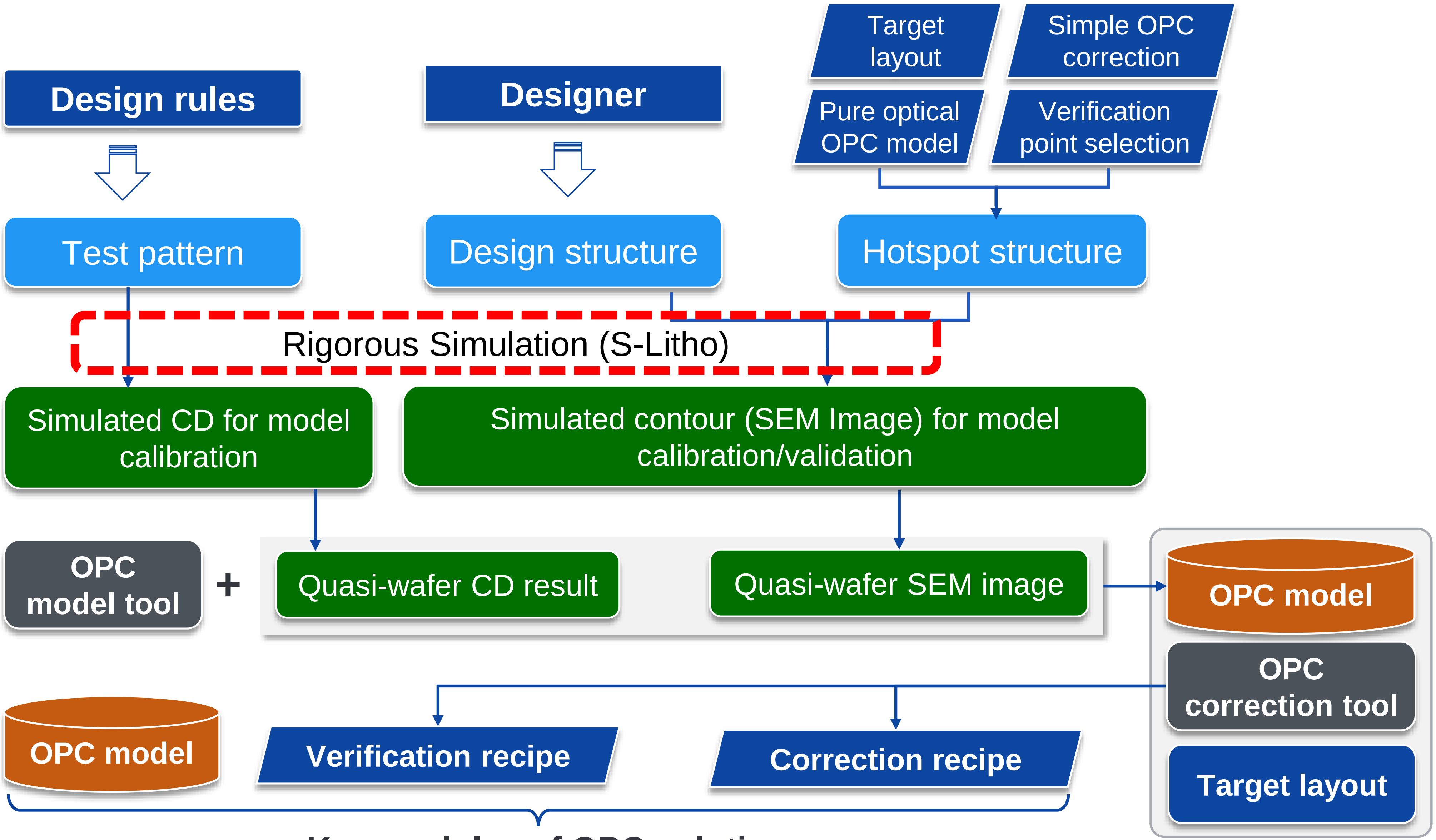
PWA

Process Window Analysis





OPC solution based on rigorous simulation



Design rules

Designer

Target layout

Simple OPC correction

Pure optical OPC model

Verification point selection

Test pattern

Design structure

Hotspot structure

Rigorous Simulation (S-Litho)

Simulated CD for model calibration

Simulated contour (SEM Image) for model calibration/validation

OPC model tool

+

Quasi-wafer CD result

Quasi-wafer SEM image

OPC model

OPC correction tool

Target layout

OPC model

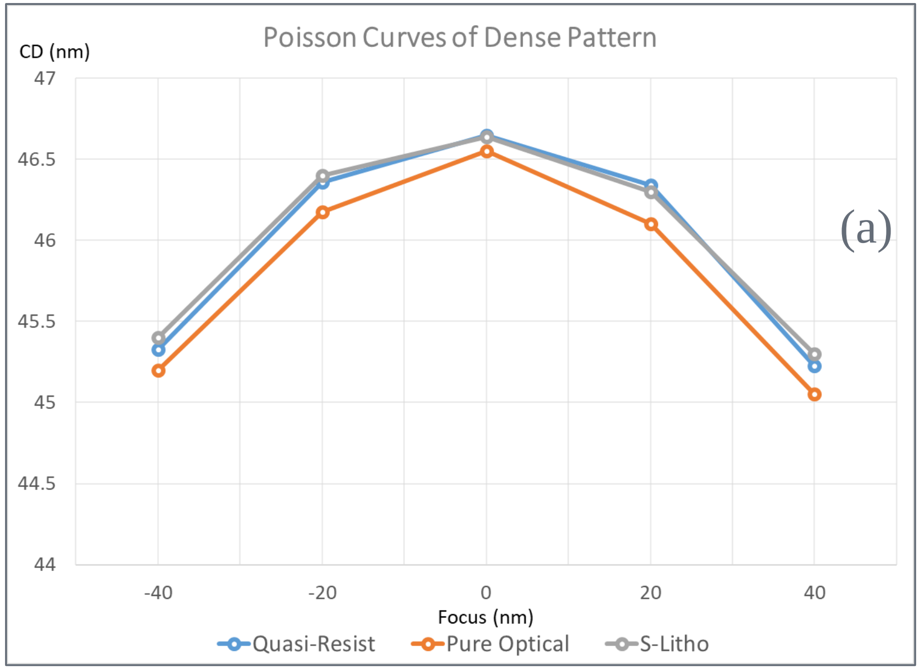
Verification recipe

Correction recipe

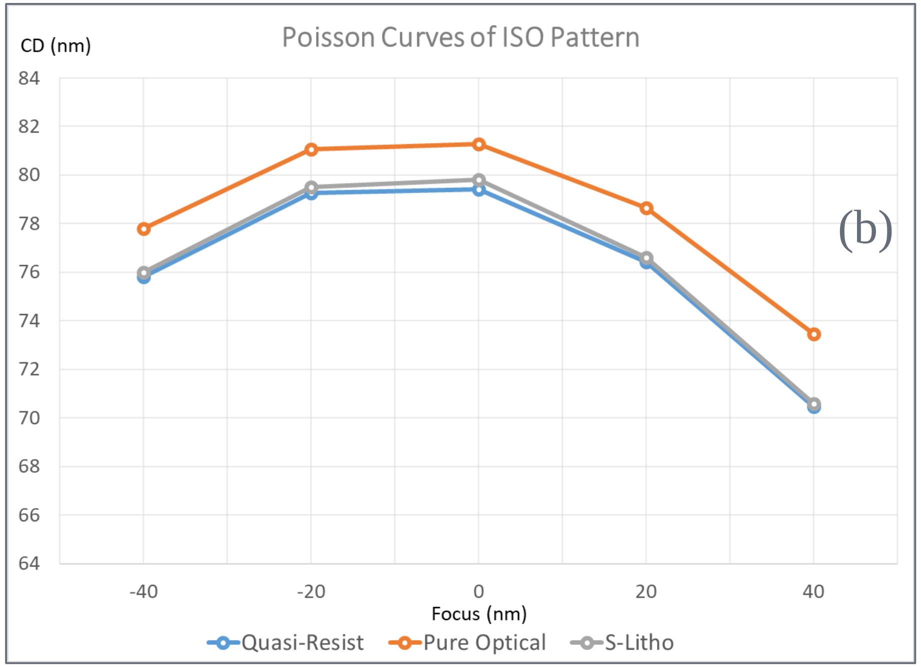
Key modules of OPC solution

Practice Case – Poisson Curve

☐ Poisson Curves of Dense Pattern



☐ Poisson Curves of ISO Pattern



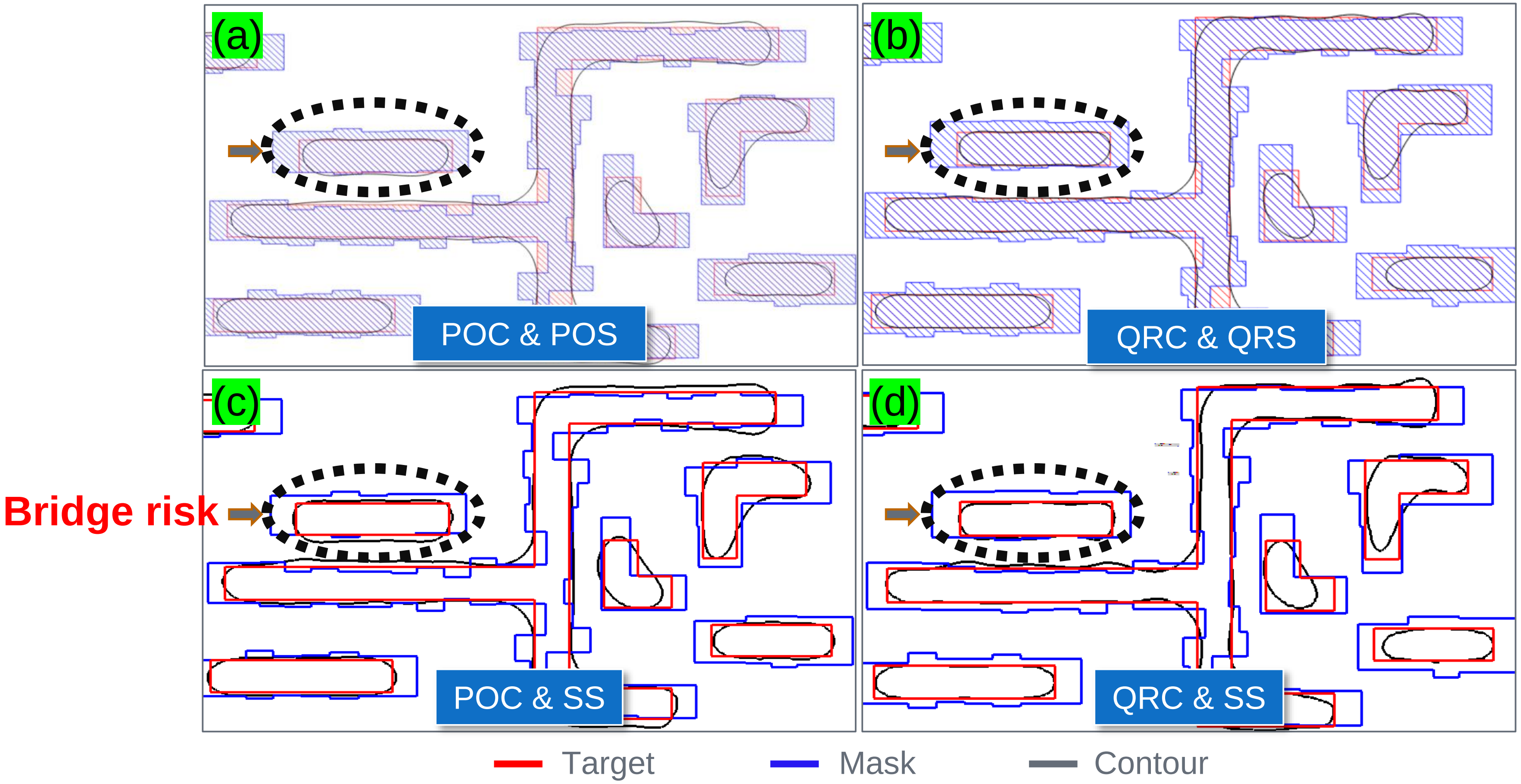
- **Quasi-Resist**: the model calibrated using quasi-wafer data by rigorous simulation
- **Pure Optical**: only optical parameters were used when building the model
- **S-Litho**: the results obtained by S-Litho software (as reference)

➢ **S-Litho is considered as an accurate model**

➢ **Results show that the quasi-resist model is more reliable**

Practice Case – Correction & Simulation

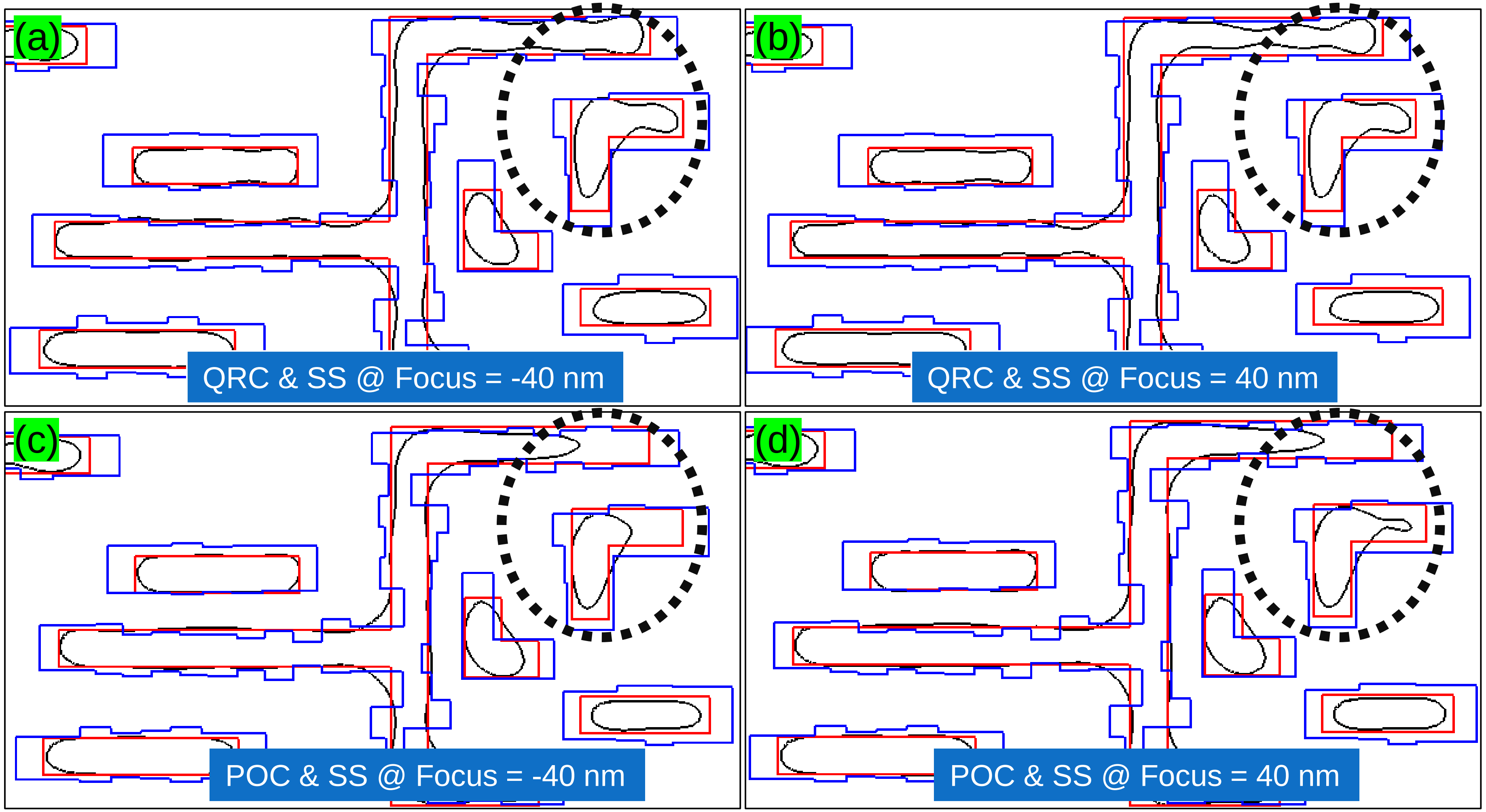
OPC corrected effect under different models



- POC: pure optical model corrected
- POS: pure optical model simulated
- QRC: quasi-resist model corrected
- QRS: quasi-resist model simulated
- SS: S-Litho simulated (**Validation**)

Practice Case - PWA

Process window analysis, focus = ±40 nm



🟥 Target 🟦 Mask ▬ Contour

Conclusion

Rigorous simulation, as a prediction and optimization tool, is of great significance in the application of lithography technology:

01

Improving production efficiency

Through rigorous simulation, the lithography effect under different process parameters can be quickly predicted, reducing the number and time of experiments in actual production.

02

Optimize process parameters

Rigorous simulation can accurately simulate various factors in the lithography process, and through the adjustment of process parameters, the optimal lithography effect can be found, improving product performance and yield.

03

Reducing costs

Through accurate simulation, the optimal lithography effect can be predicted during the experimental stage, reducing waste in actual production and lowering production costs.

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Thank You!

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