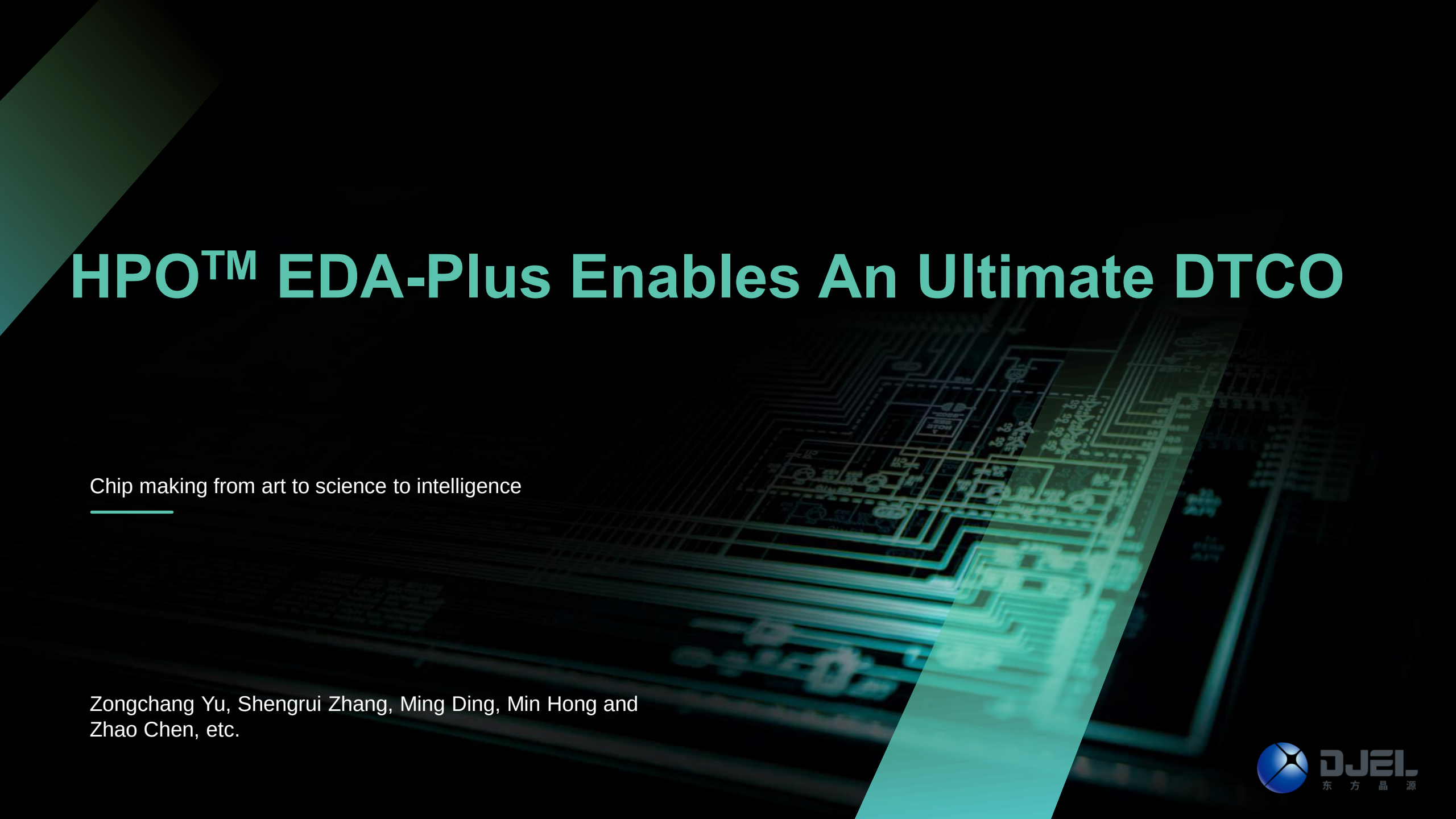
HPO™ EDA-Plus Enables An Ultimate DTCO

Chip making from art to science to intelligence

Zongchang Yu, Shengrui Zhang, Ming Ding, Min Hong and Zhao Chen, etc.



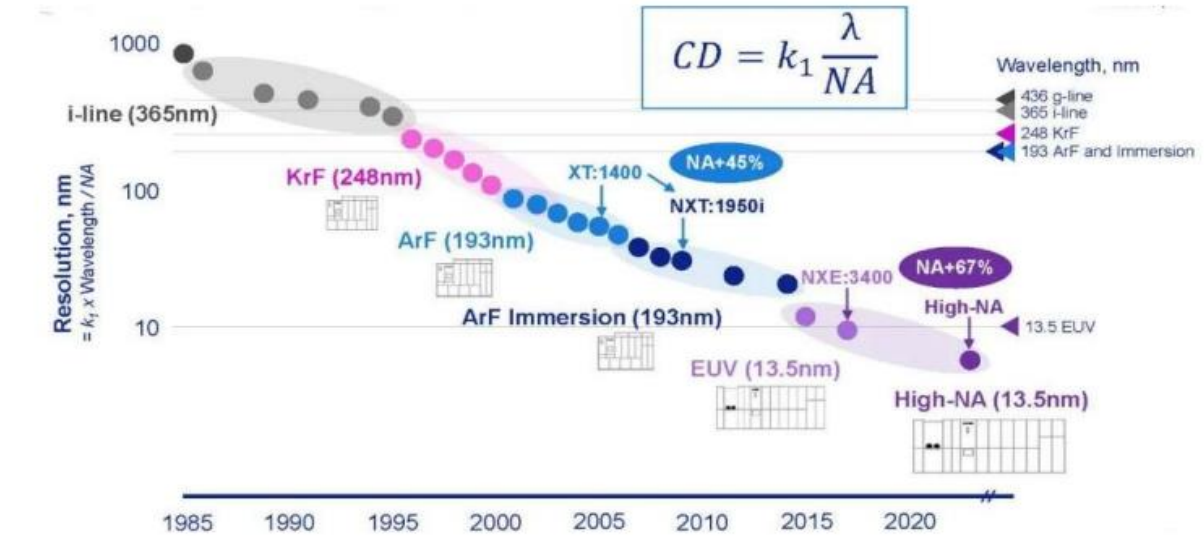
Outline

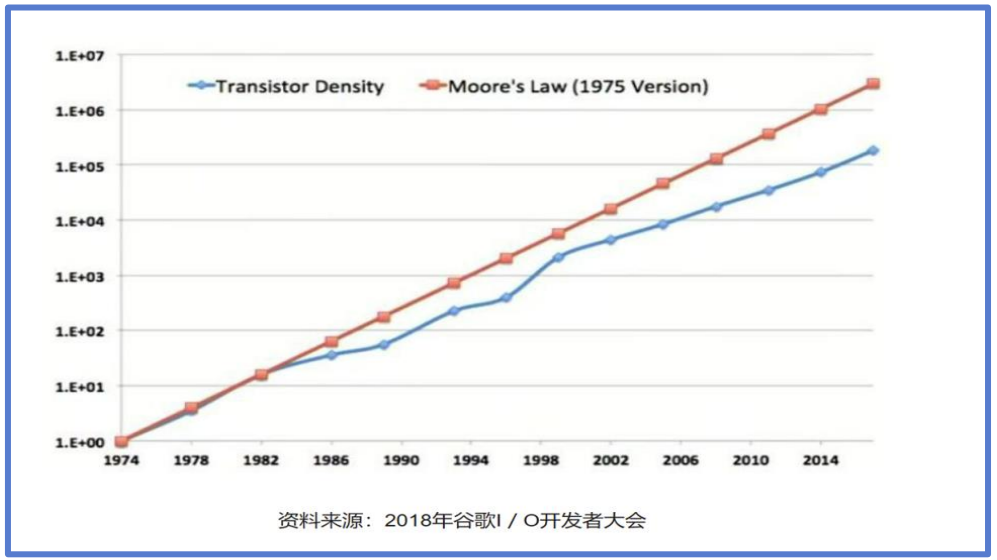
Slowing down in Moore's Law, More than Moore

Extending Moore's law by upgrading hardware has hit physical or economic limitations:

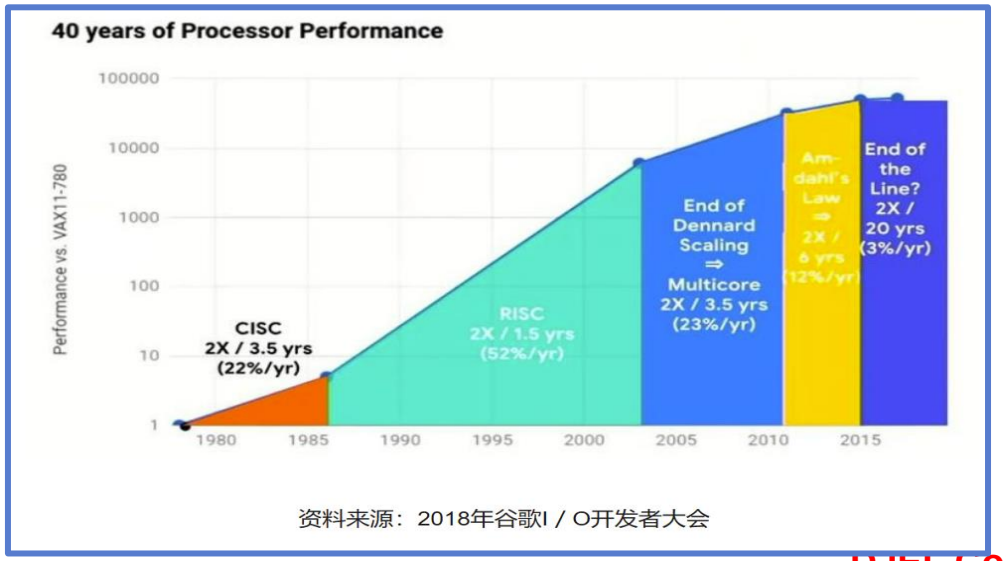
- **Making of "point tools" has become more challenging.**
- **IC manufacturing processes have become more and more complicated and expensive .**
- **The Result: monopoly in IC supply chain, winners take the largest profit.**

EUV: Only one vendor !
Hardware based Moore's Law is ended. Crisis, but also opportunity for Holistic Process Optimization !





资料来源：2018年谷歌I / O开发者大会



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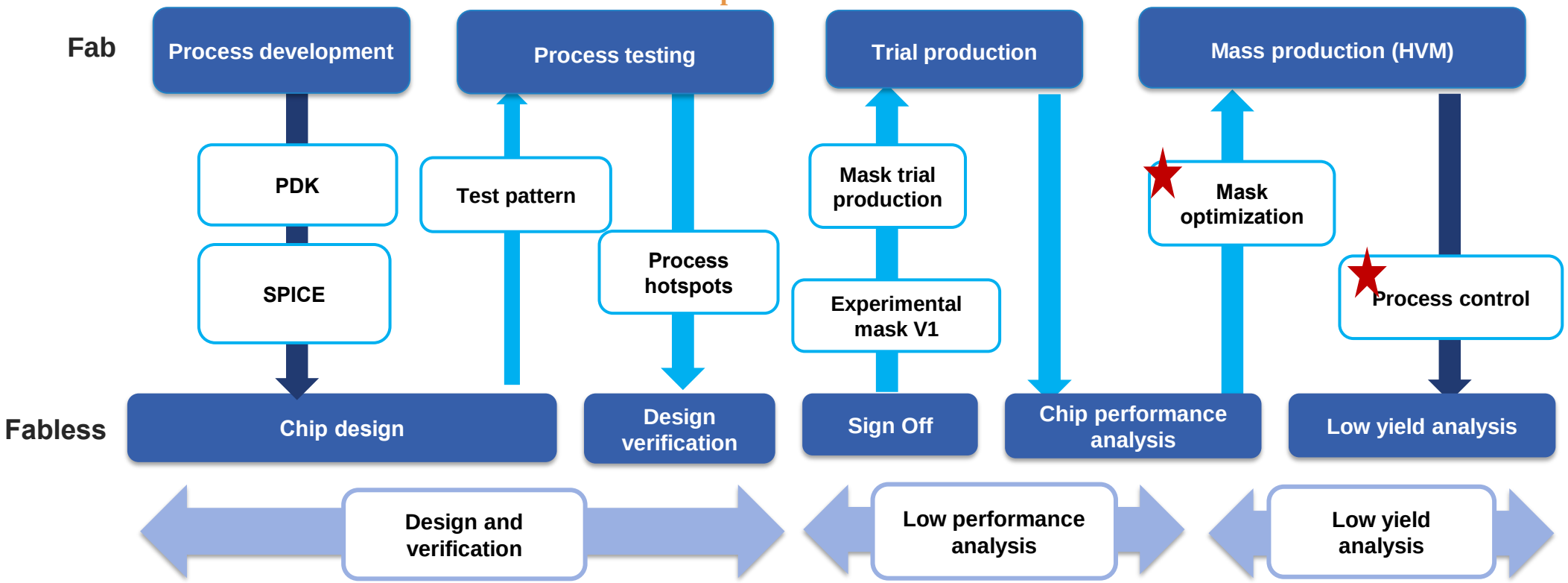
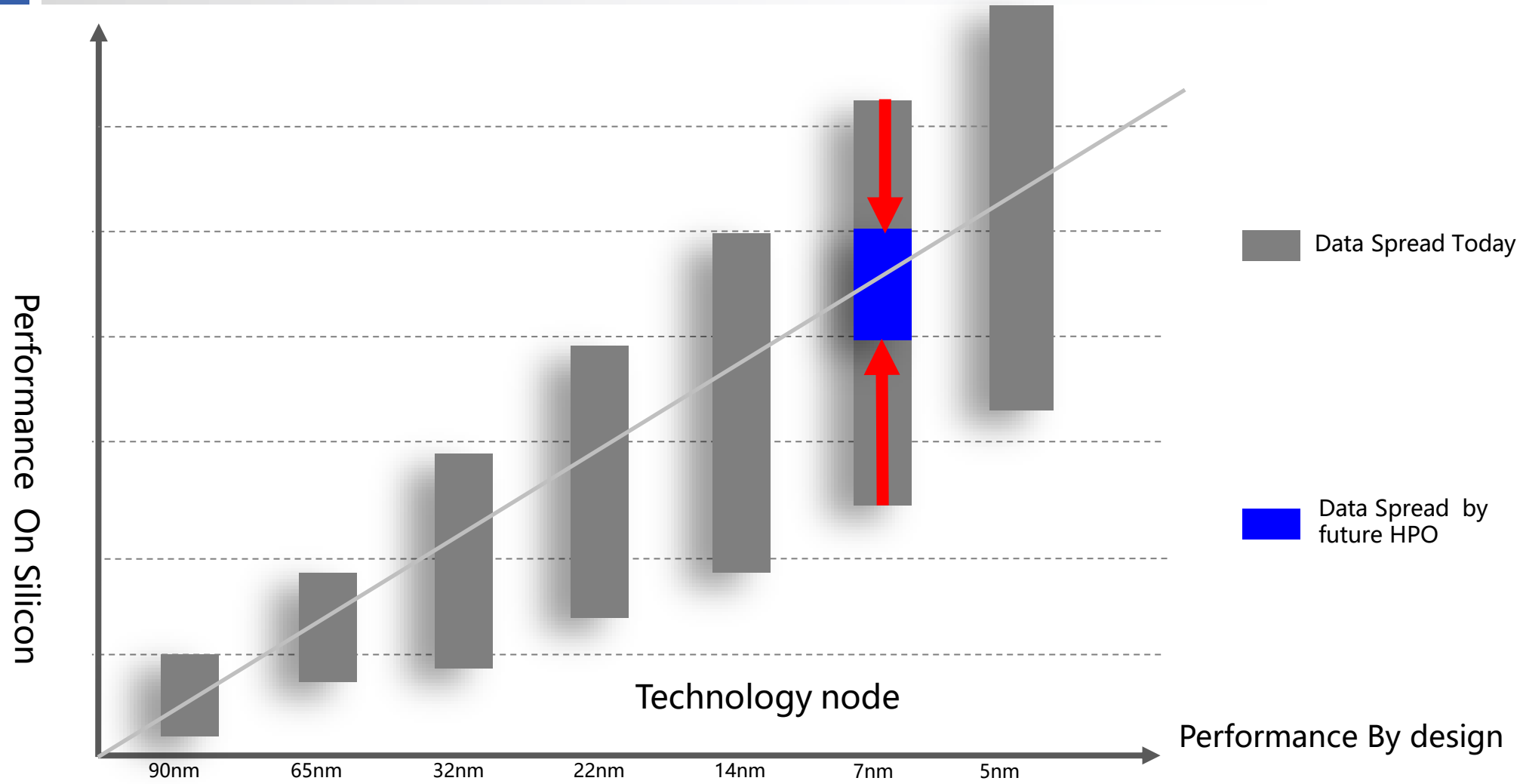
Complexity and pain points in design and manufacturing CoOp

Data sharing and comprehensive optimization of design and manufacturing are the key to shorten R&D cycle and achieve yield up and cost down



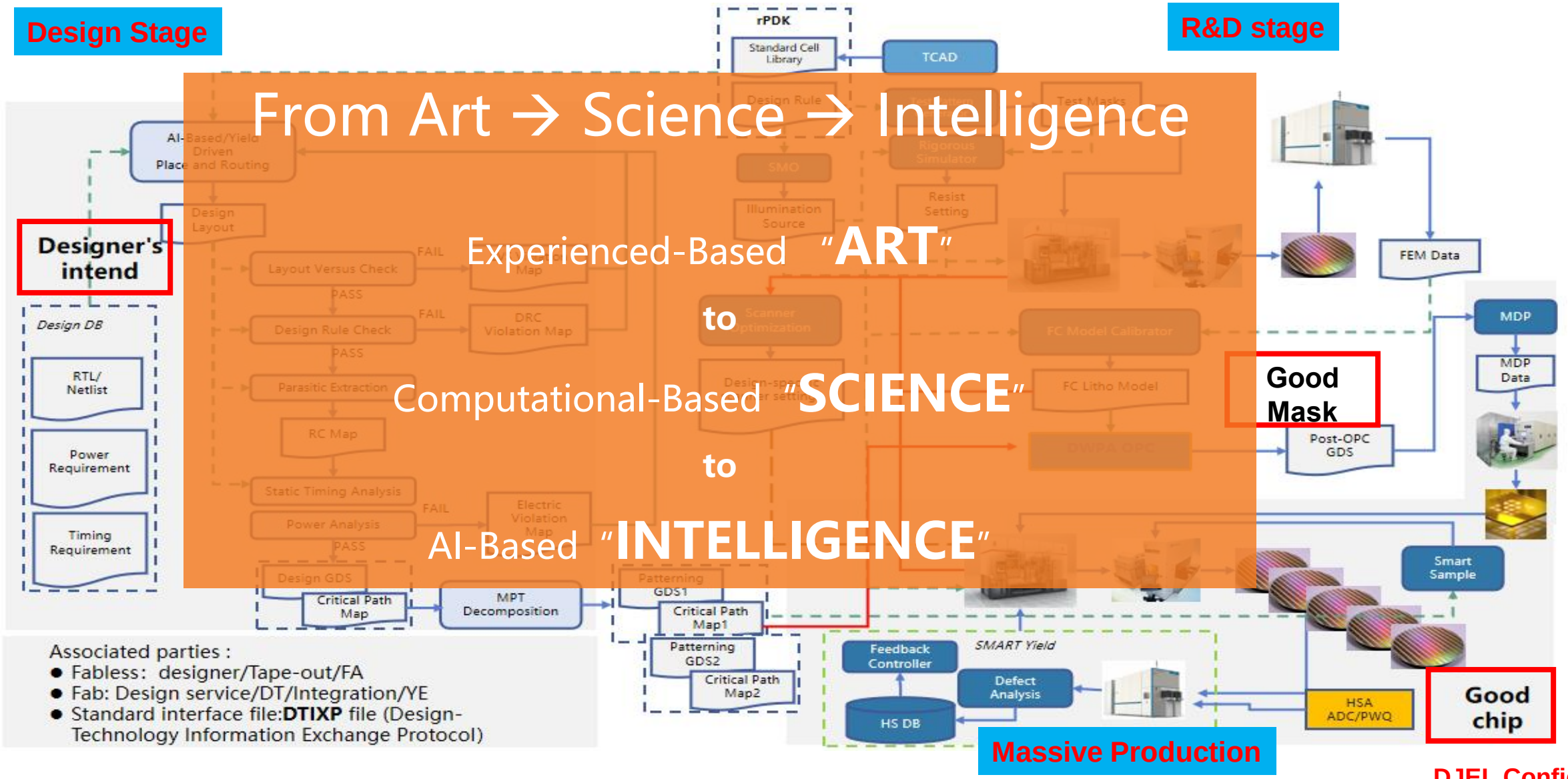
- Complex of processes involving multiple parties
- Amount of data related to process quality reached humongous level beyond capacity of current system
- The PDK no longer accurately and timely represents the manufacturing capacity of a given fab
- Yield is heavily rely on engineers' experiences in both fab and in fabless

Yield predictability becomes key factor of shortening R&D cycle



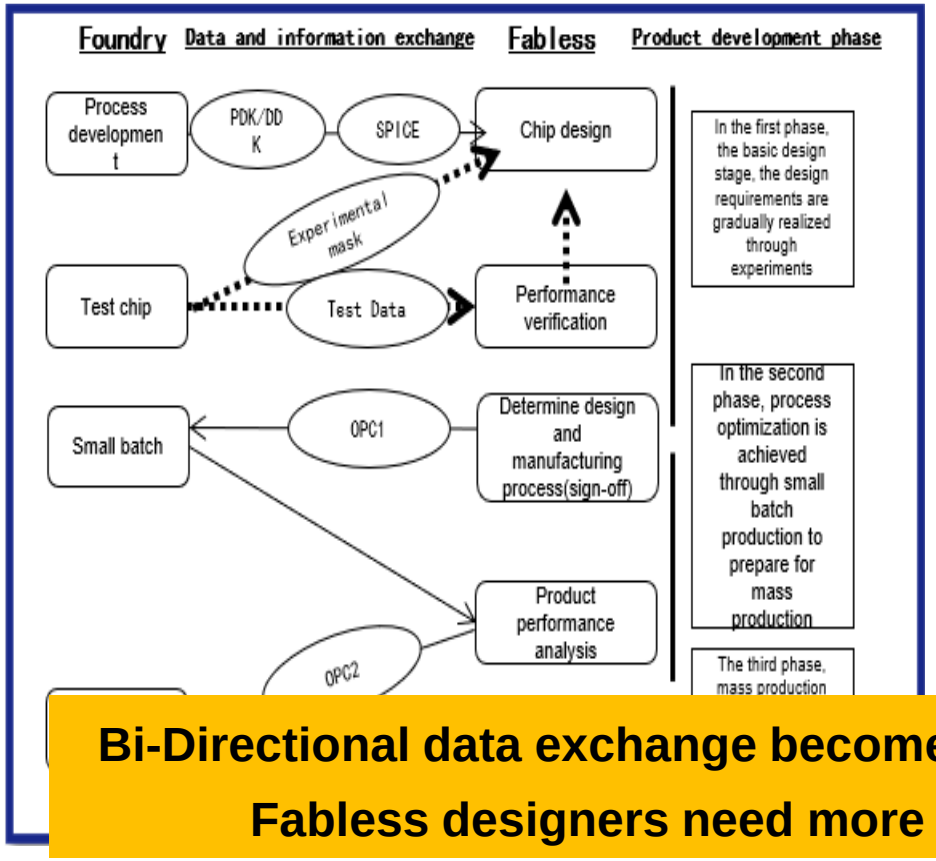
- Large spread of measured vs. designed resulting more iterations, longer yield ramping, eventually increasing chip cost and time-to-market.
- Also small spread means possibility for less matured tech node to support better chip performance

Achieving an AI-Based Ultimate DTCO Flow



Outline

HPO™ : Seamless connection between design and manufacturing, platform for an ultimate DTCO



The basic functional modules of HPO™

- Feedforward（Yield Optimization）：Design for yield
- Feedback(Design Optimization)：Design optimization based on inspection and big data analysis, reduction in design iterations.
- HPO™ connects design data, process modeling and inspection data, makes data exchange easier for DTCO （Design-


证书号第3313833号

发明专利证书

发明名称：一种大规模集成电路设计和制造的综合优化设备及方法

发明人：俞宗强;李江伟

专利号：ZL 2015 1 1019096.7

专利申请日：2015年12月30日

专利权人：东方晶源微电子科技（北京）有限公司

地址：100176 北京市北京经济技术开发区经海四路156号院12号楼

授权公告日：2019年03月29日　　授权公告号：CN 105740496 B

国家知识产权局依照中华人民共和国专利法进行审查，决定授予专利权，颁发发明专利

商标注册证

HPO

注册日期 2017年12月28日 有效期至 2027年12月27日

局长 刘俊臣 发证机关 商标局

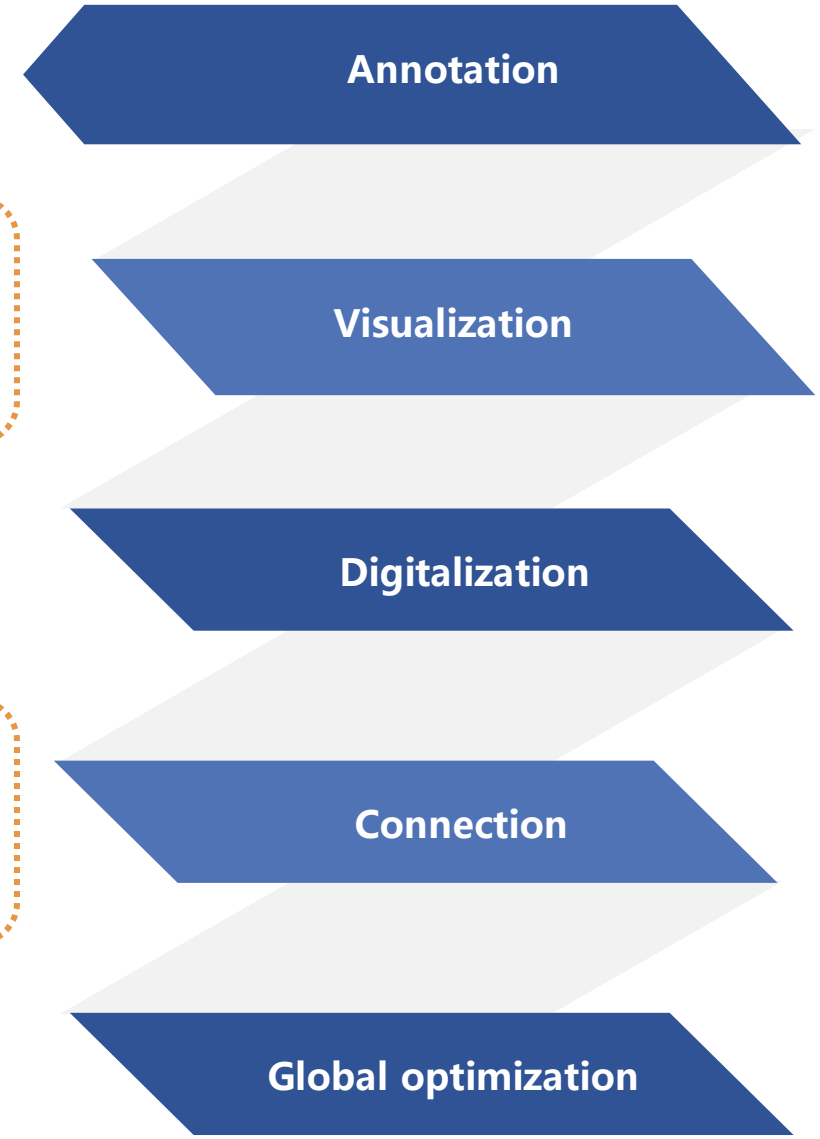
Bi-Directional data exchange becomes increasingly important as design rule shrinks!

Fabless designers need more visibilities inside the manufacturing floor!

China patent: A comprehensive optimization equipment and method for design and manufacture of large-scale integrated circuits,

Application Number：CN201511019096.7， Application date ：2015.12.30， Priority date：**2014.12.31**

Key Components: Making yield computable, visible, measurable, globally optimal



Design, manufacturing and yield management use an uniform language and measure for optimization scoring

Nano-meter resolution imaging system + inspection/metrology algorithm in manufacturing processes

Simulation, modeling and libraries for emulating physics in IC making

Seamless connection between processes virtually through cloud or other platforms

Maximize usage in huge amount of data during process through out design and manufacturing processes

Foundation and tools for establishing the HPO™ Platform

EBI

SEpA ixx series SEM products
Available for 28nm devices used in physical and VC defect inspections.
Enable visualization in chip making

CD-SEM

SEpA cxx series SEM products:
Available for 28nm devices.
Under evaluation at an advanced foundry
Enable visualization in chip making

DR-SEM

SEpA rxx series SEM products:
Available for 3D-NAND、DRAM devices
Under evaluation at an advanced foundry
Enable visualization in chip making

DJEL is a only company that provides P&R、OPC、 Metrology/Inspection and Yield Management system and tools， this uniqueness allow us to do things differently.

Place & Route

HXOPT full flow P&R tool:
Comparable PPA to commercial tools,

Enable optimization and connection in chip making

OPC/RET/oDAS

PanGen series computational lithography products:
adopted by advanced **IDM and foundries.**
Enable digitization、optimization and connection in chip making

YieldBook

Defect Management System
Yield Management System
Design Based Measurement, Inspection and Defect Analysis
Enable annotation and connection in chip making

Holistic Process Optimization: EDA-Plus & CM/I

RTL/Netlist

Floorplan

Placement

CTS

Routing

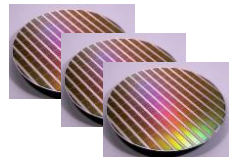
STA

Sign Off

Design GDS

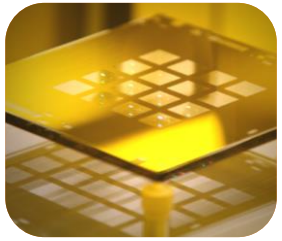
Yield BOOK

EBI CD-SEM DR-SEM

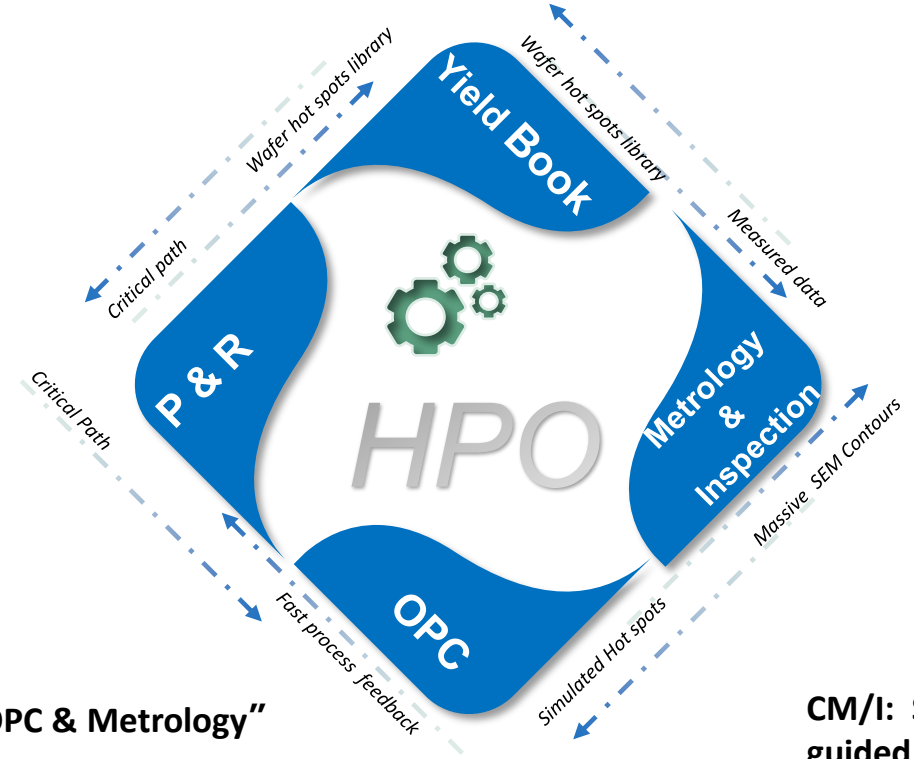


Optimize Process Params

SMO



Making Reticle



EDA+ : "P&R + OPC & Metrology"
→ True DTCO !

CM/I: Smart Metrology guided by design and OPC

Modeling

MPT

Mask Optimization

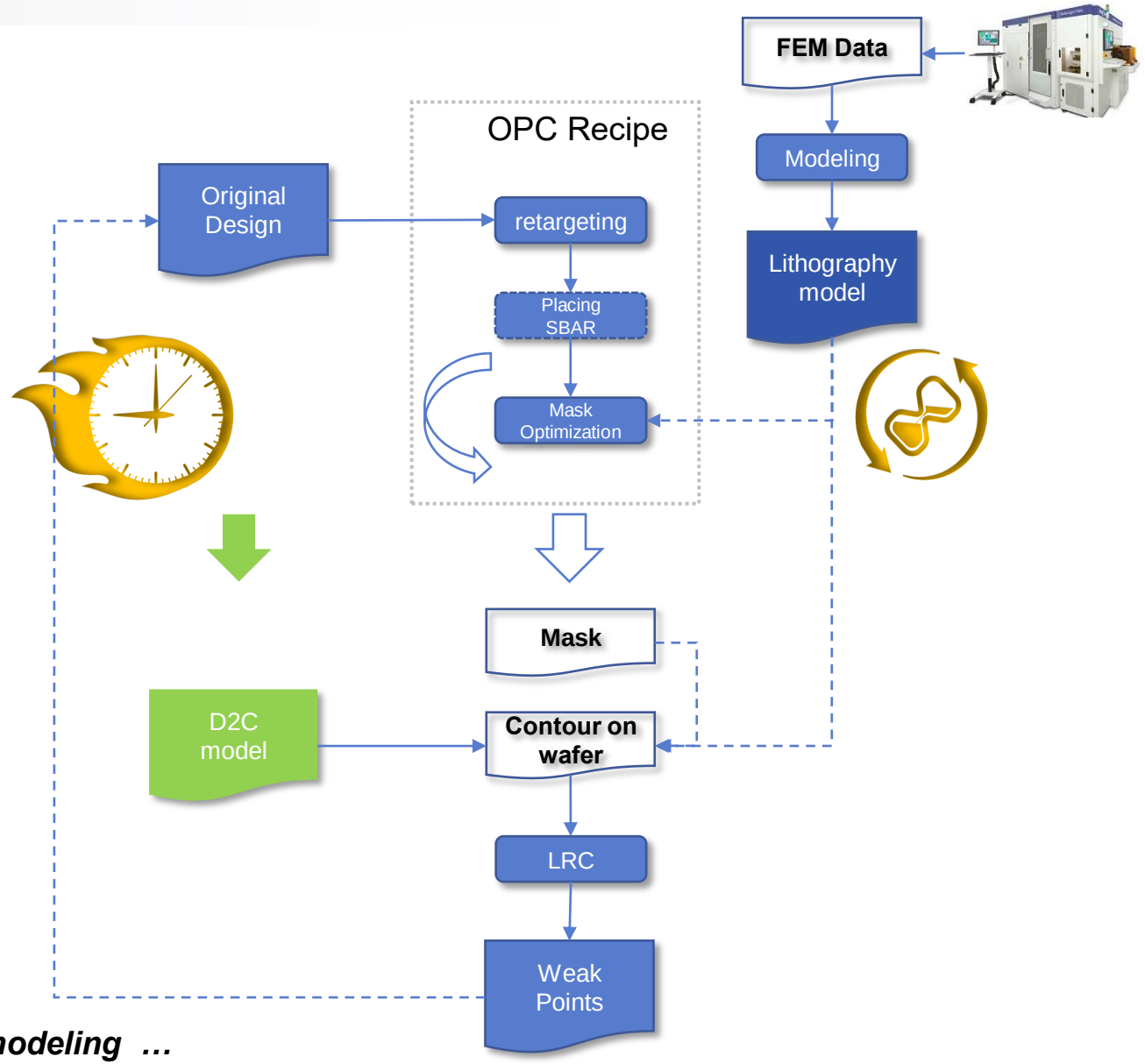
LRC

MDP

Outline

D2C：Fast Feedback From Process to Designer

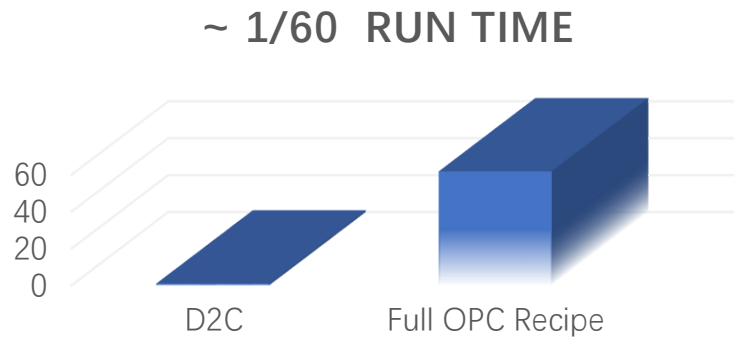
- Obtain accurate ADI contour from original design
- Fast and direct lithography feedback to designer
- Seamlessly integrated with PanGen OPC Platform
- D2C AI model can be directly calibrated based on PanGen full chip OPC solution

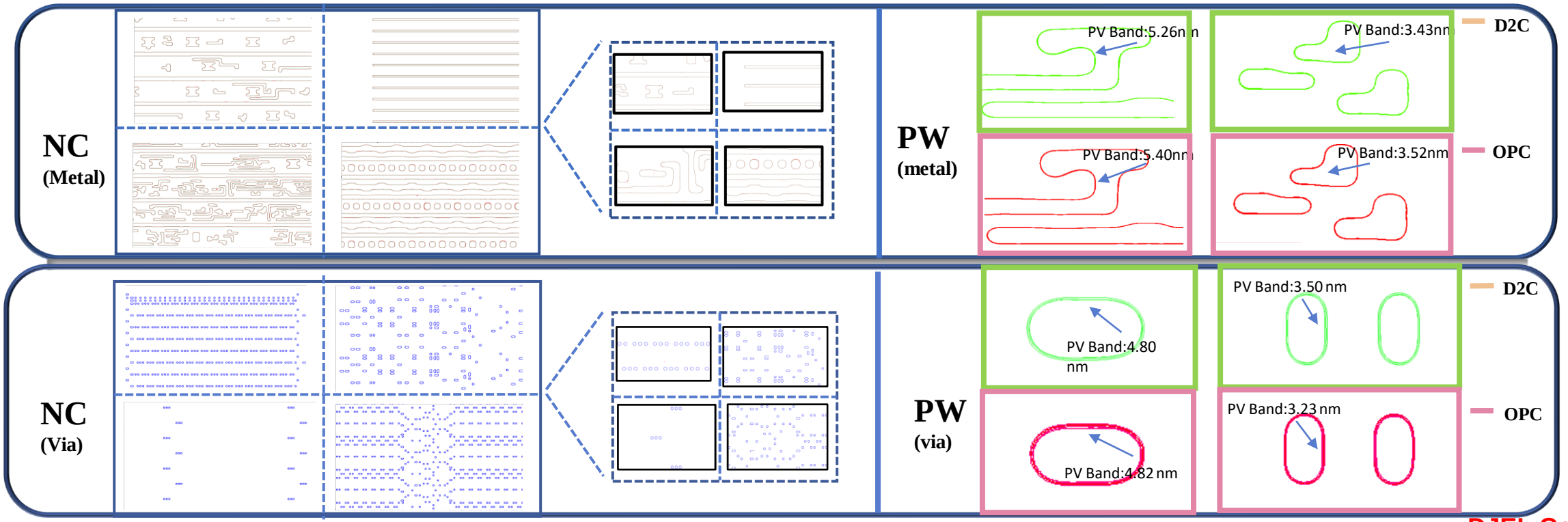


Note: D2C can further extend to etch modeling and HotSpot modeling …

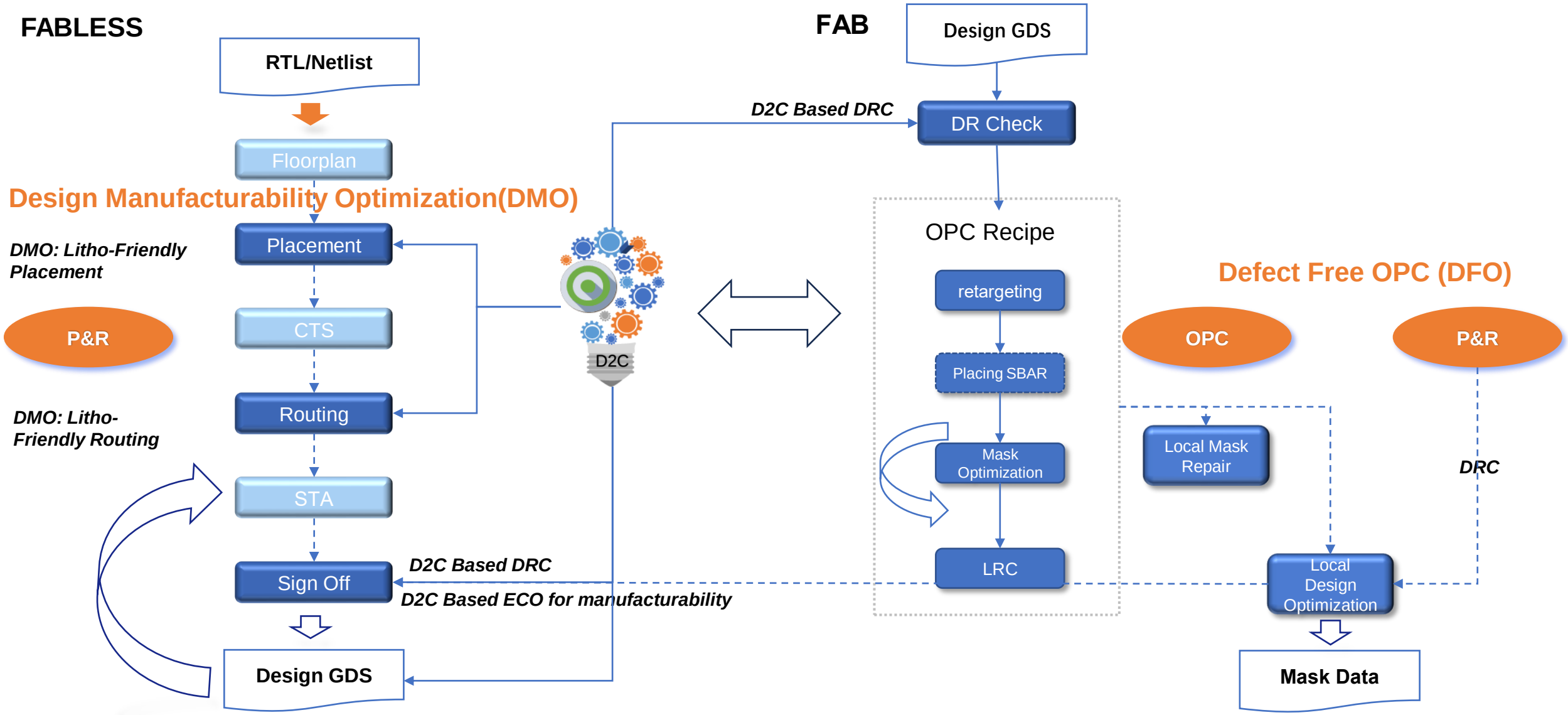
Accurate and Fast Lithography Feedback

NO.	Simulation Condition	GDS SIZE(um)	Accuracy (nm) (Sigma of the Contour to Contour Differences)	LRC Defect Count (With FAB sign off spec)
1	NC	4000*4500 (Full Chip Xiangshan 28nm) 	0.63	0 (Same Sign off LRC results)
2	NF40		0.64	
3	PF40		0.65	
4	PD+3%		0.67	
5	ND+3%		0.65	

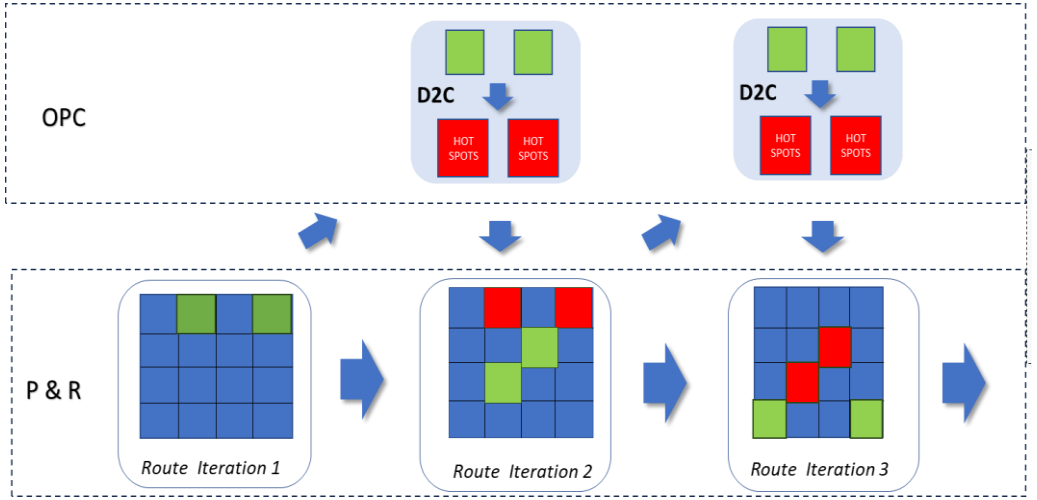


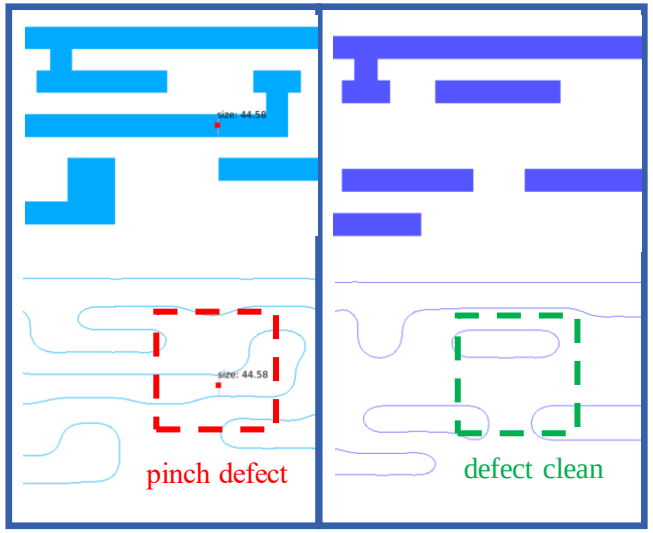


HPO™ EDA-Plus: From DMO, DFO to TAR

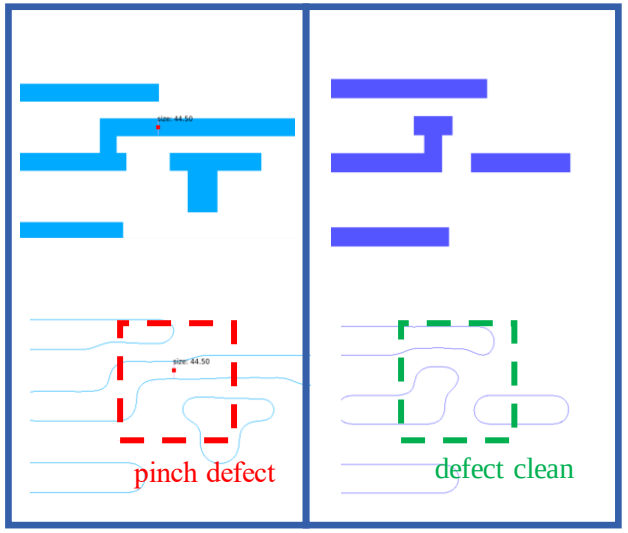


HPO™ EDA-Plus improves the Yield





Baseline ⇨ *Rerouted*



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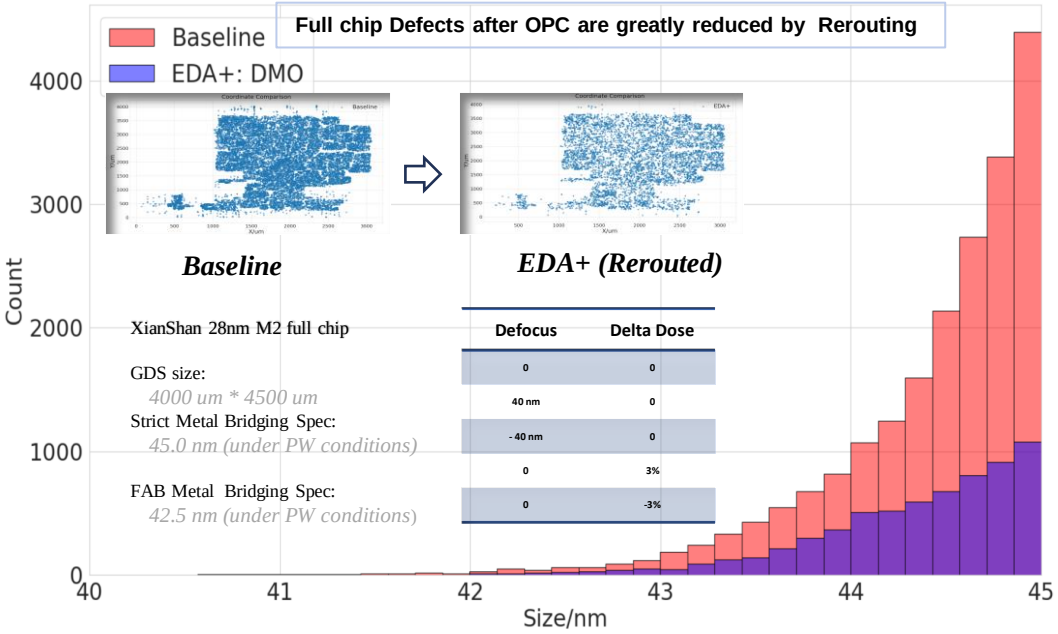
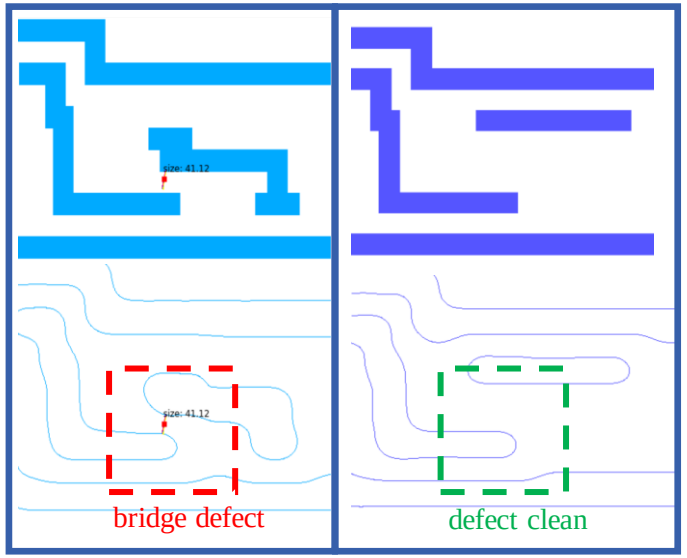
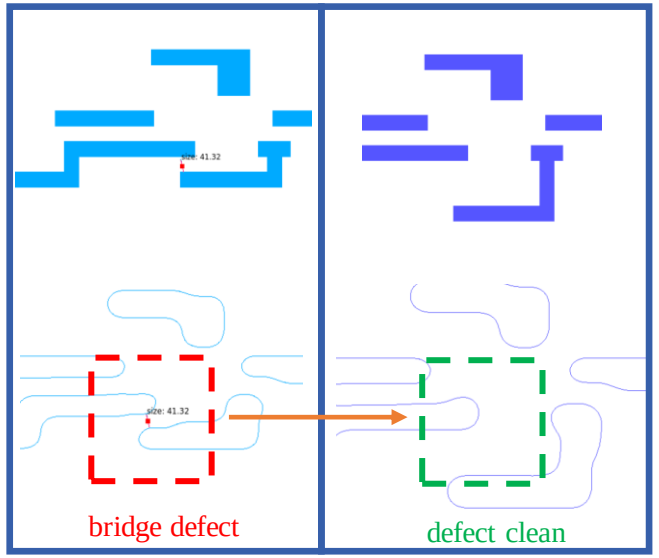
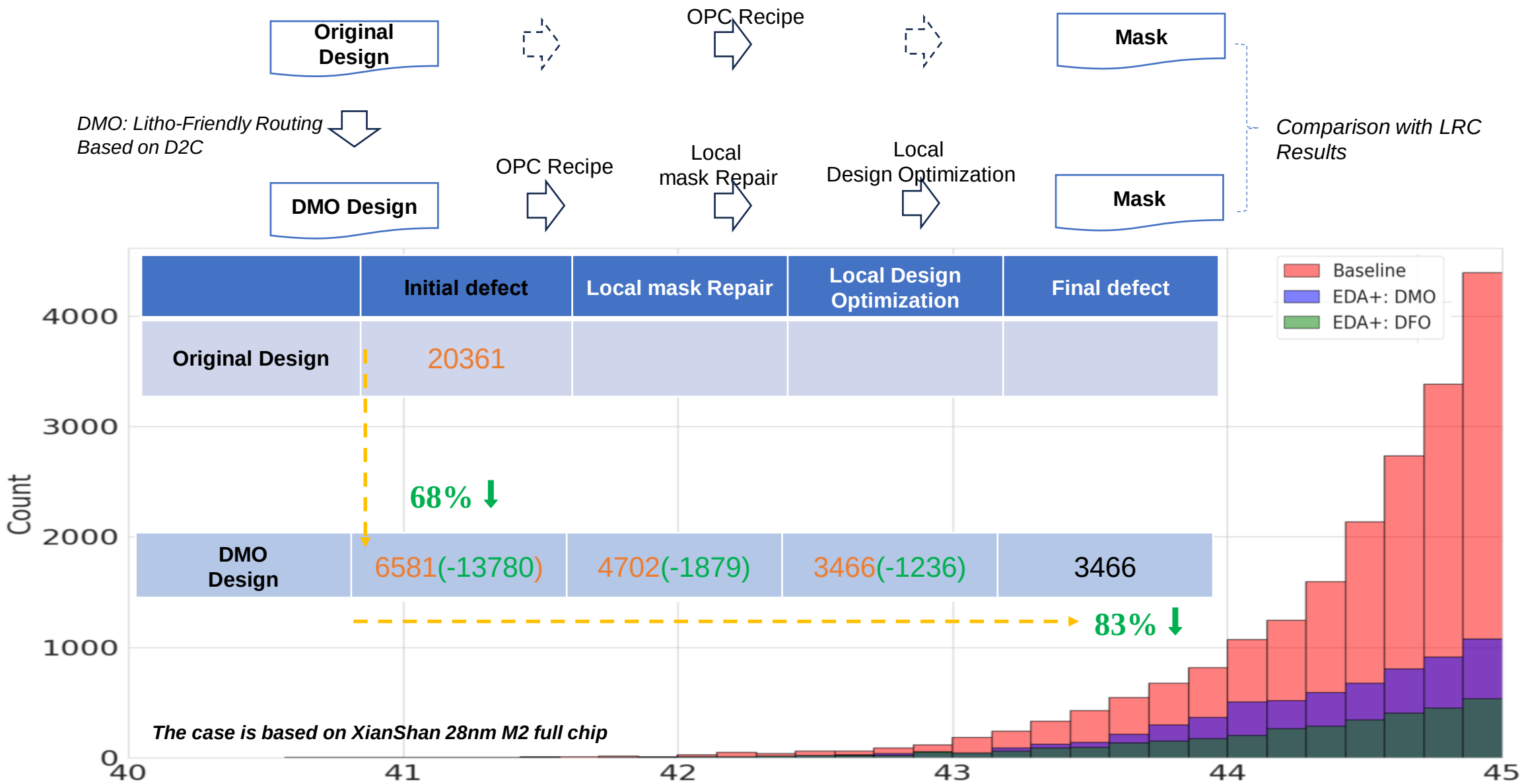


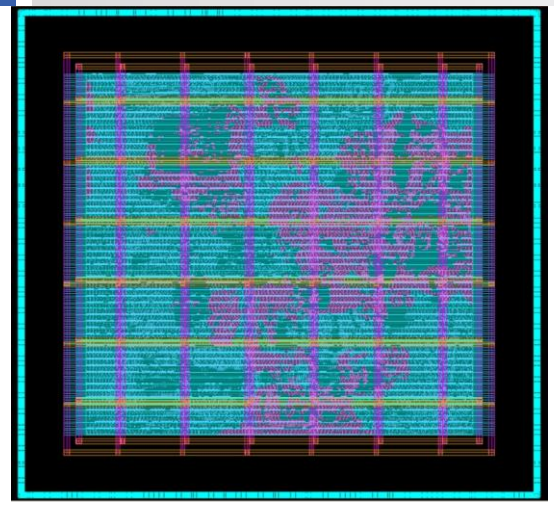




HPO™ EDA-Plus improves the Yield cont

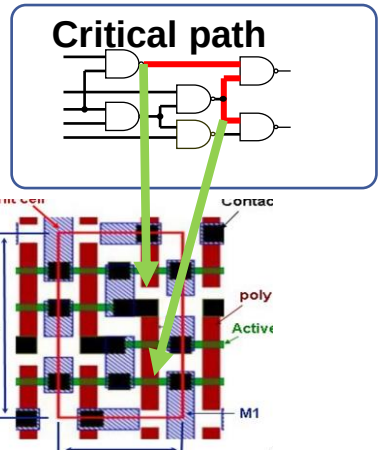


HPO™ EDA-Plus improves the chip performance



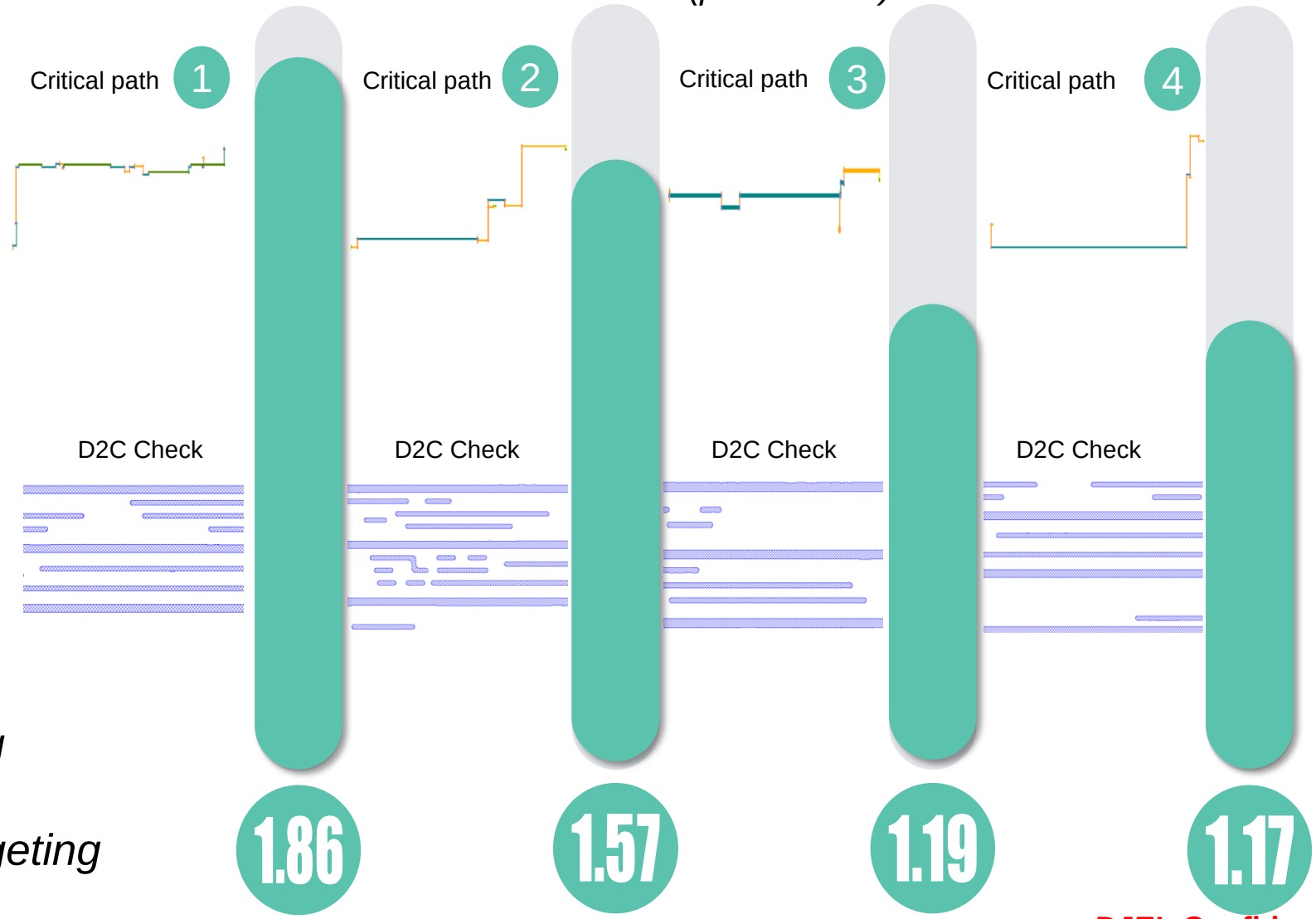
300u *300um
Chip Size

75232
Instances



Timing Aware Retargeting

Timing Improved for the critical paths
(picosecond)



Outline

01 Challenges and opportunities in IC Making

02 Introduction to HPO™ EDA-Plus

03 Practice on HPO™ EDA-Plus: DMO, DFO, TAR

04 Conclusions

HPO™ EDA-Plus: Designer's Intend To Good Chip (D2GC)

- Slowing down of Moore's law provided opportunities for innovation in advanced IC Making
- HPO™ EDA-Plus platform enables seamless connection between design and manufacturing to achieve ultimate DTCO, and AI-Based Chip Making
- HPO™ EDA-Plus has show promising results in improving yield and chip performance
- We will continue our efforts to add more tools in HPO™ EDA-Plus system, finally build an innovative infrastructure for Yield up & Cost Down in IC making

THANKS ALL

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