Control Strategy for Improved After-Etch Overlay at Wafer Edge of DRAM Layers in High-Volume Manufacturing

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Outline

- Background introduction
- Benefit of control strategy (scenarios & simulations)
- Conclusion
- Q & A

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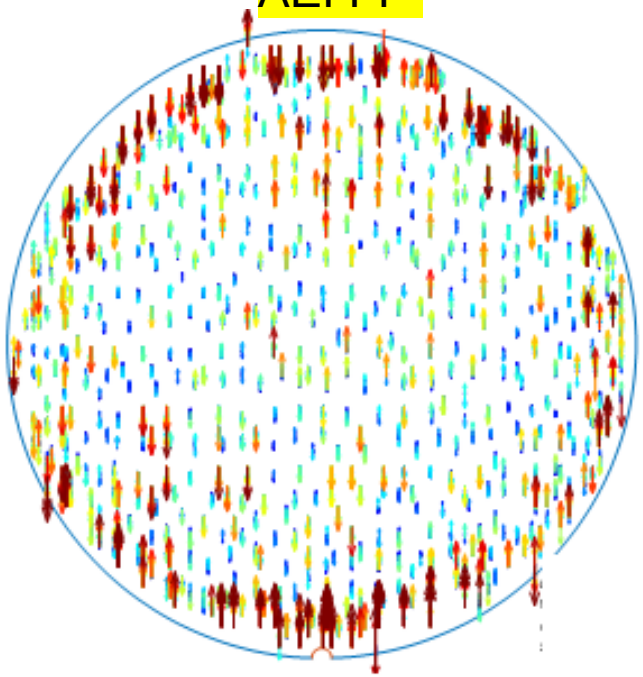
Background introduction

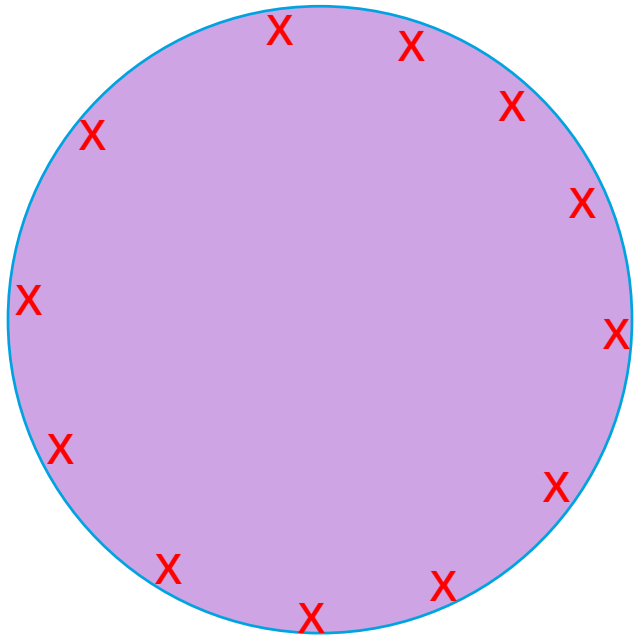
- CXMT sees severe edge AEI OVL can often lead to edge yield loss

AEI FP



Large OVL at wafer edge

Yield map



Yield loss at wafer edge

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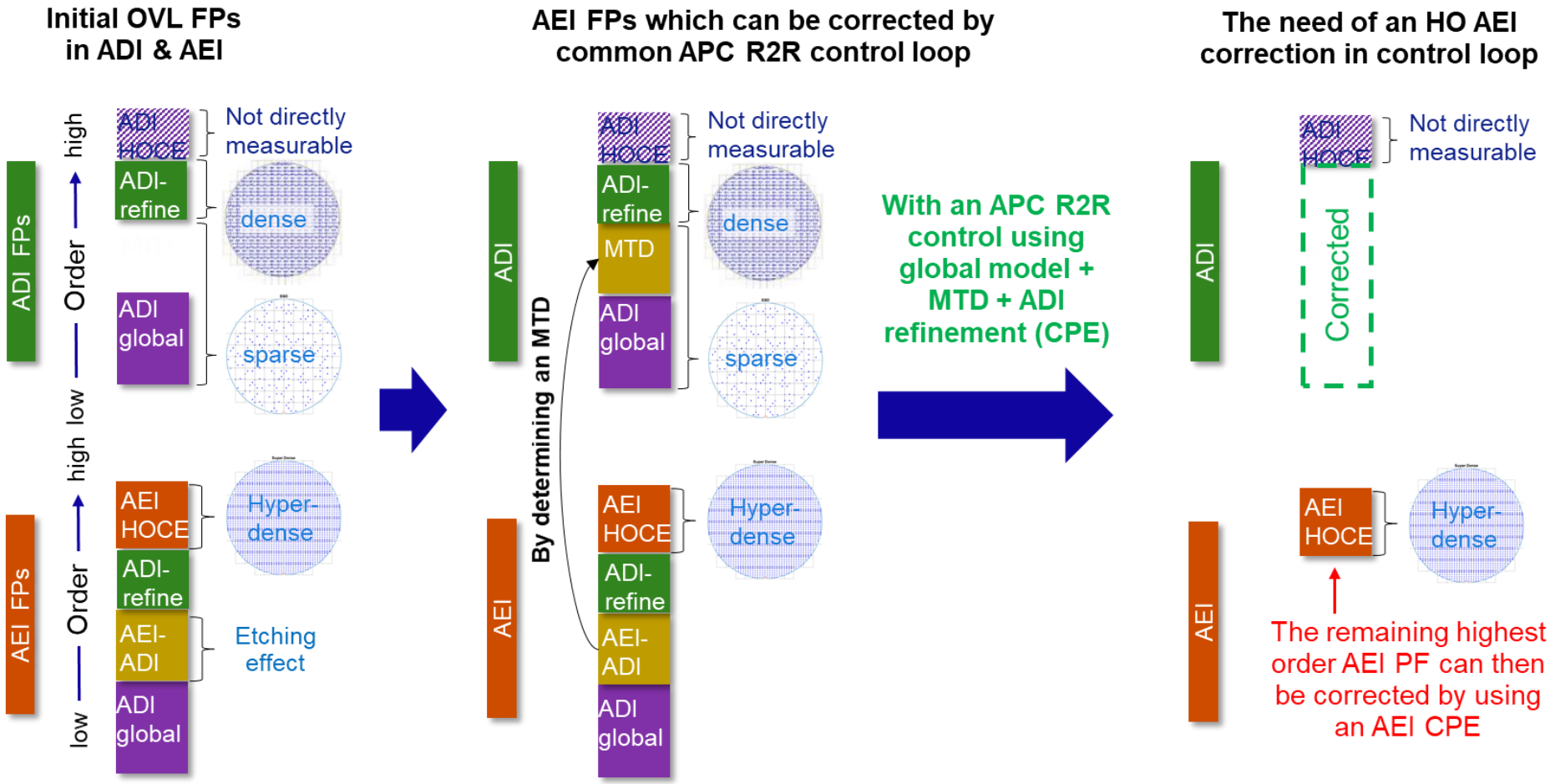
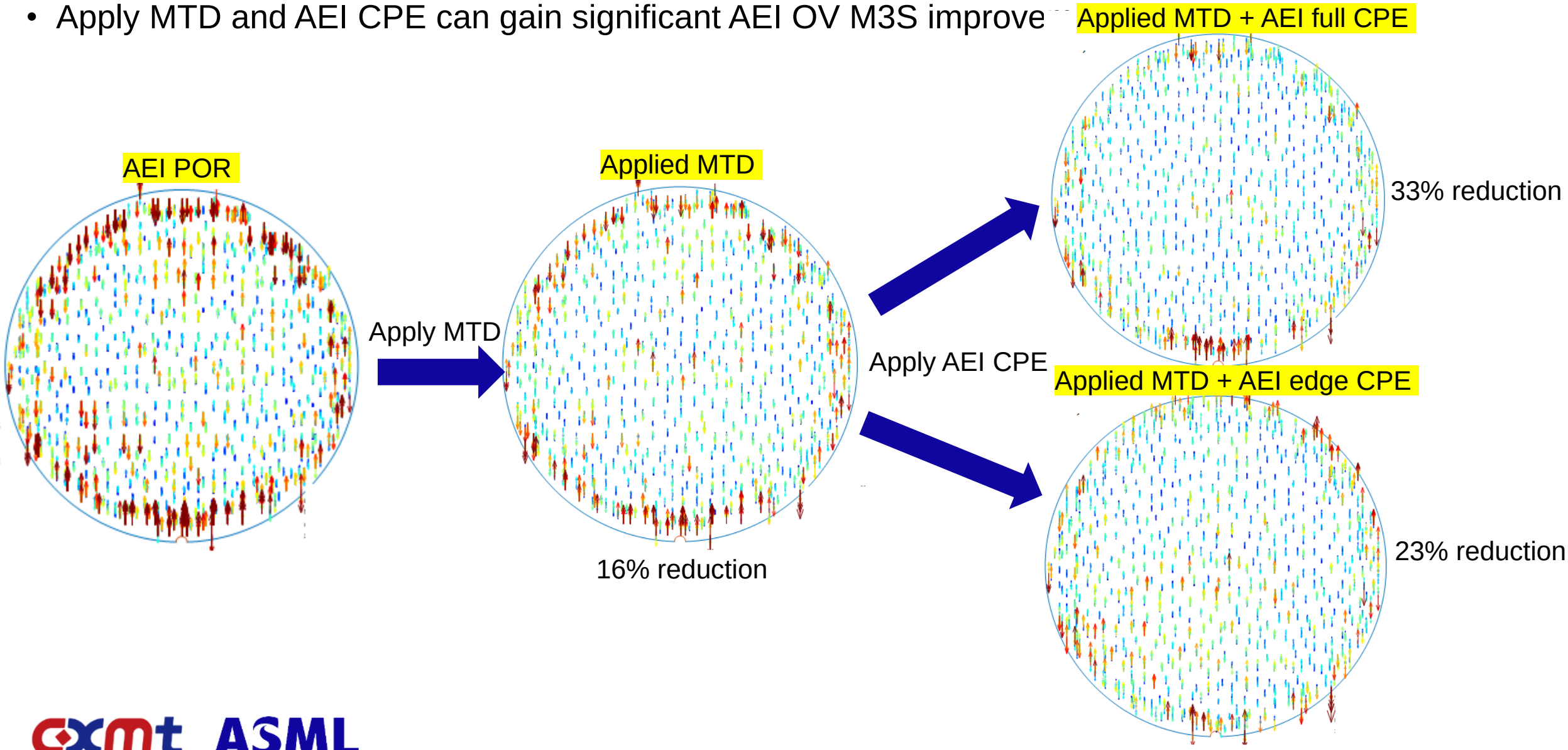
Overlay components in ADI and AEI, and their corrections in control loop

- Conventional APC control loop needs to be extended to cover high-order AEI fingerprint



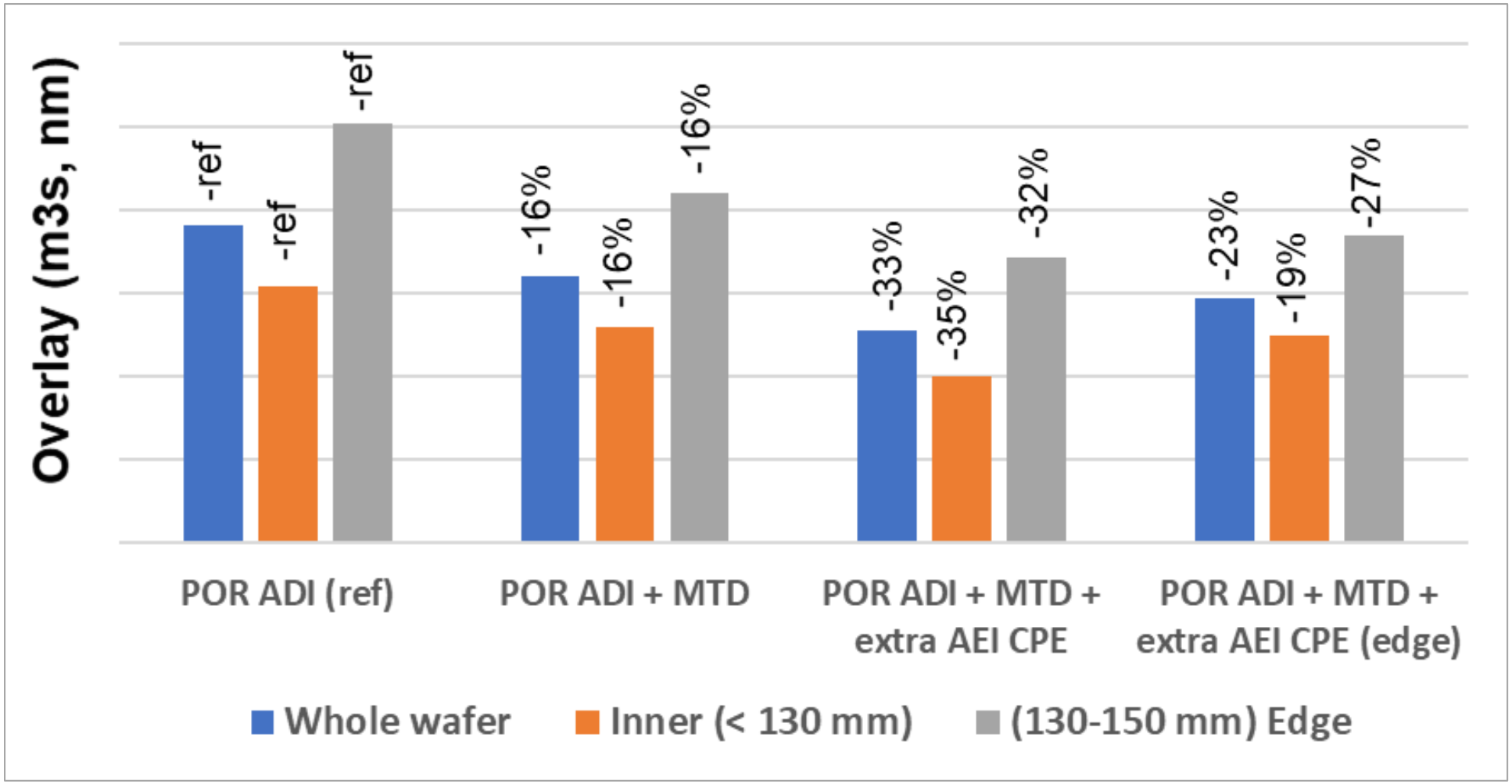
Global MTD + AEI CPE simulations

- Apply MTD and AEI CPE can gain significant AEI OV M3S improve



AEI OPO gains by different control scenarios

- Gain at edge vs inner: about similar % for both, but much larger in term of nm for edge



cxmt ASML

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Conclusions

- **Critical DRAM layers could suffer from larger after-etch overlay at wafer edge area. A common practice of adding a global MTD is helpful, but it may not be enough for edge area due to high order nature of the FP there.**
- **By adding an extra AEI CPE on top of control loops of ADI APC and MTD in several scenarios, we showed that this approach is very effective in reducing AEI overlay of the addressed layer for full wafer and especially for the edge area.**
- **By this way, we expect higher yield can be achieved for critical DRAM layers, especially at wafer edge area.**

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