Pattern Centric Machine Learning Approach to Uncover Process Defects During Wafer Inspection and Review

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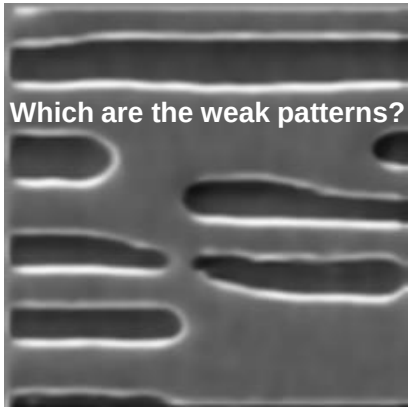
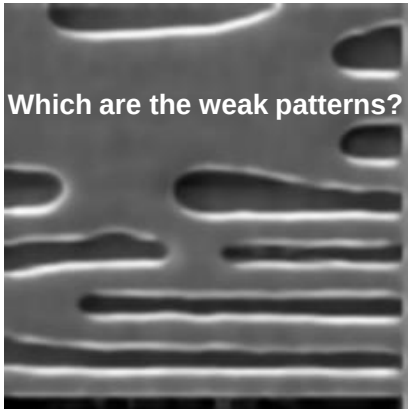
Problem Statement

- Difficult to manually identify weak patterns based on study of defect Review SEM images
- Tedious to manually check the fix of known weak patterns by guided care area inspection

Incumbent default tool challenges:

- Cannot analyze multiple layers to study full chip design
- Cannot auto analyze SEM images to reliably identify weak patterns



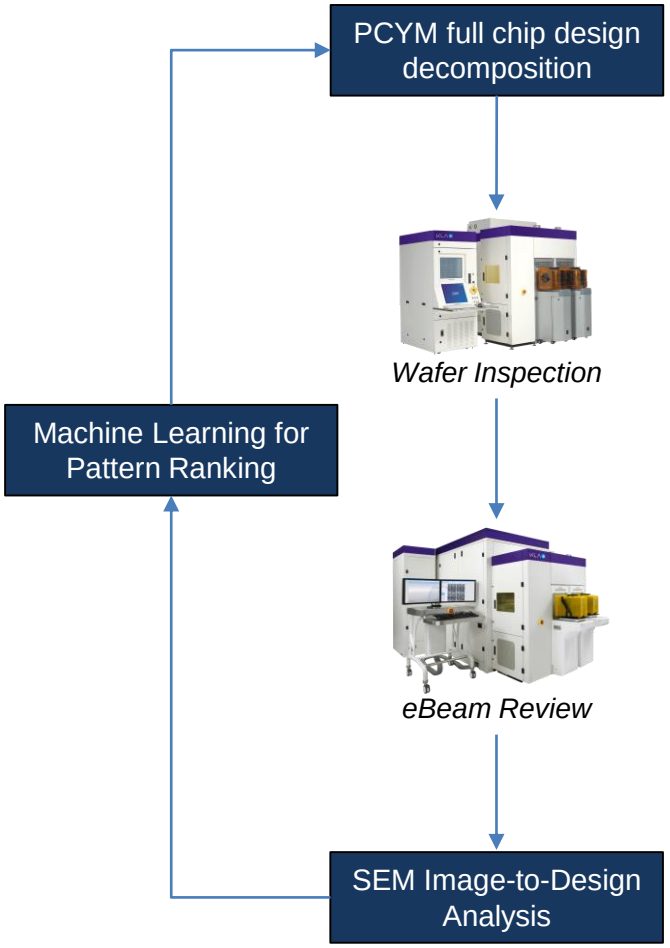


Solution

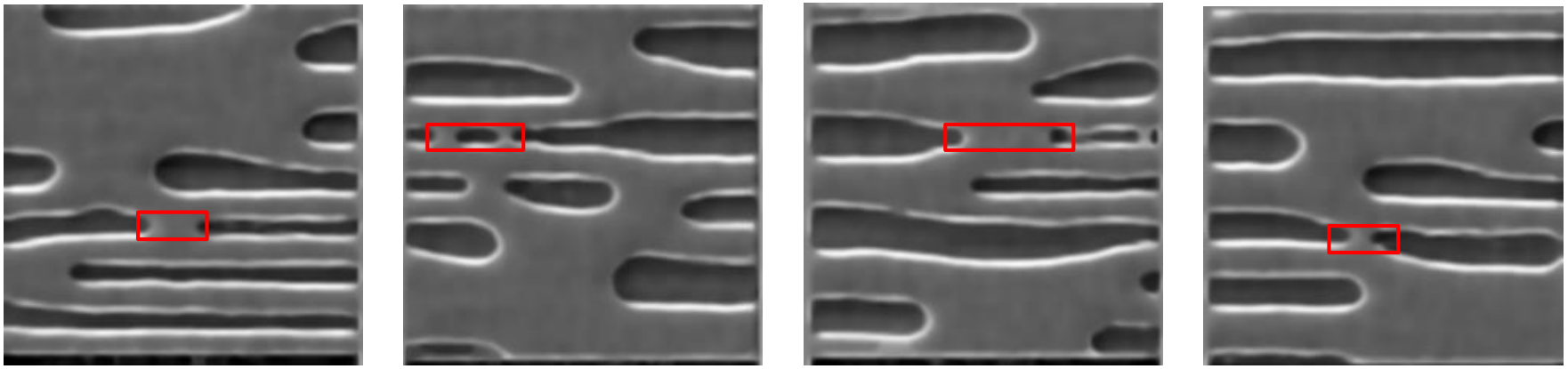
- Review SEM images guide in rule setup for full chip design decomposition and build Pattern Centric Yield Manager Database
- SEM image-to-design analysis perform automated image measurements at target locations to correlate with design and identify weak patterns
- Design and SEM image information enable pattern centric machine learning to rank patterns in PCYM DB and thereby improve sampling

Customer Success:

- Optimized pattern sampling by automated pattern analytics
- Capability to detect and monitor pattern defects with full chip coverage



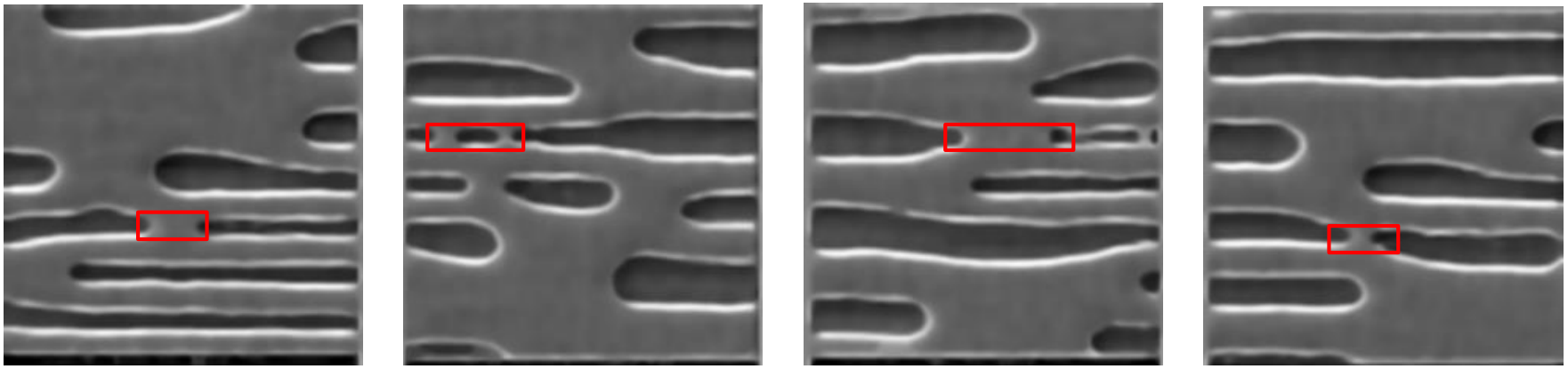
Studying Review SEM images



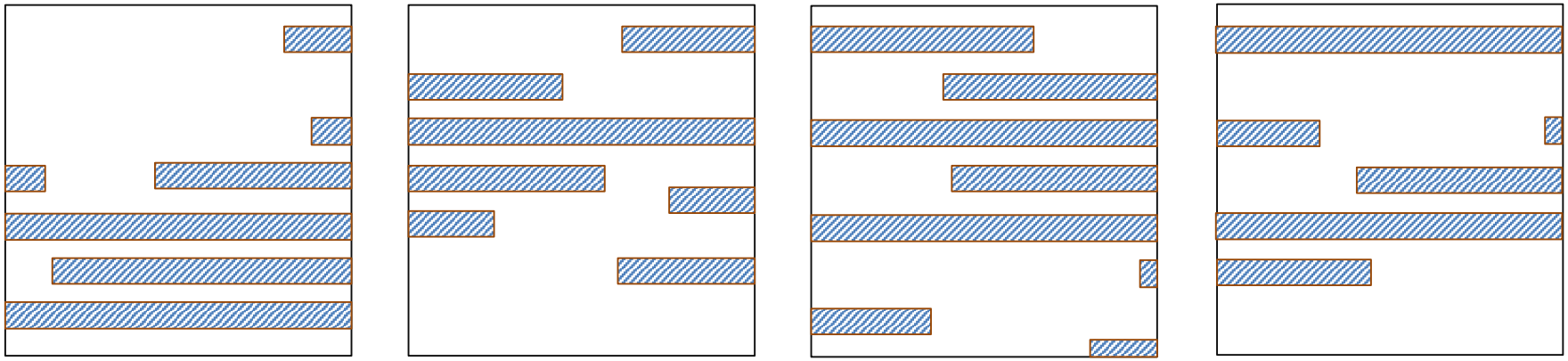
- Manual identification of matching with design clip is tedious

AEI Image Defect Center

Studying Review SEM images



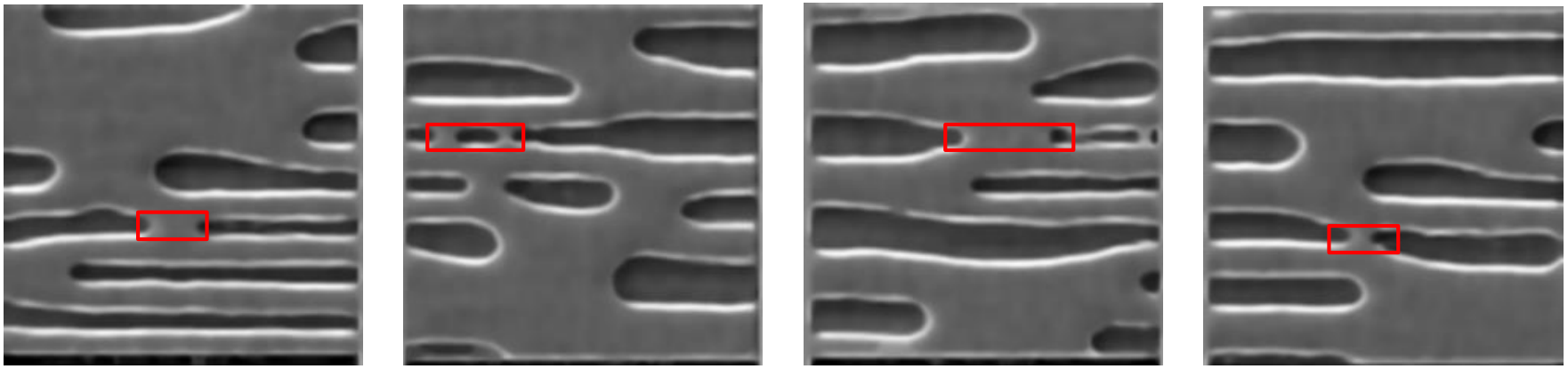
- Manual identification of matching with design clip is tedious
- Visual comparison of SEM image with single layer design does not reveal actionable information



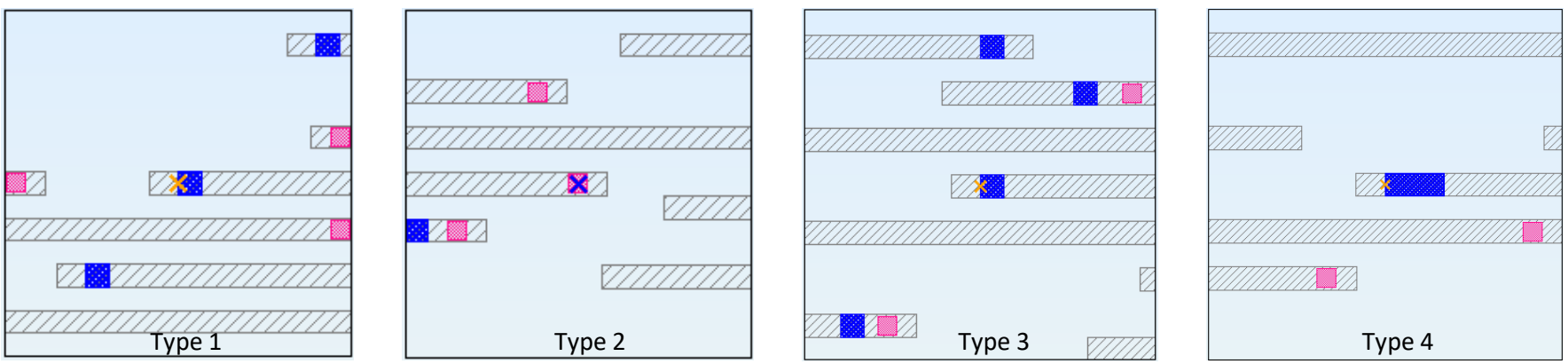
AEI Image Defect Center

$Metal_n$

Studying Review SEM images



- Layer stack around the defect location does indicate pattern correlation
- Defects occur on long metal polygons that are surrounded by line-ends and is in the vicinity of upper or lower Via



AEI Image Defect Center

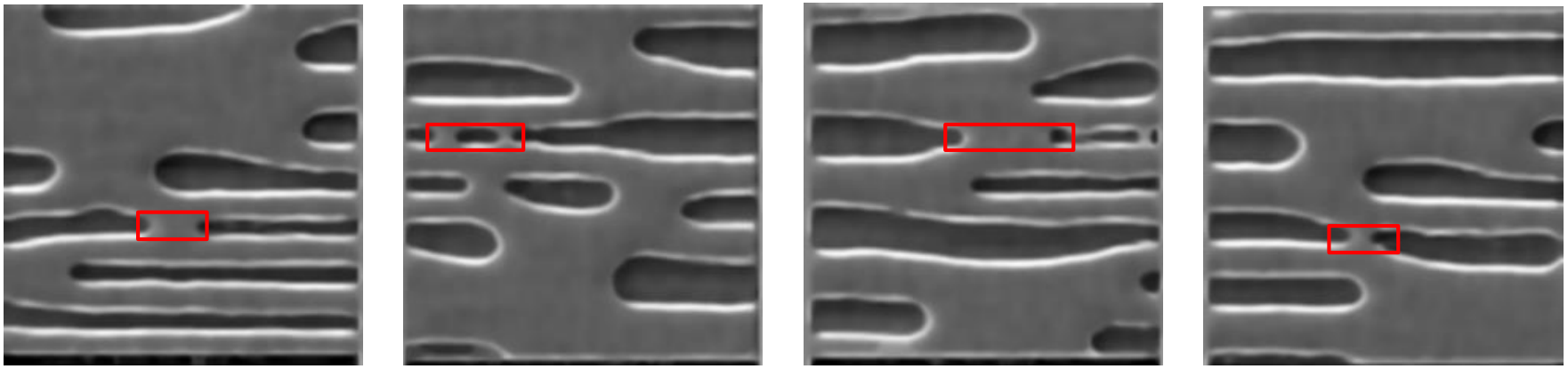
X Pattern Rule Center in PreOPC design

$Metal_n$

Via_{n-1}

Via_n

Studying Review SEM images



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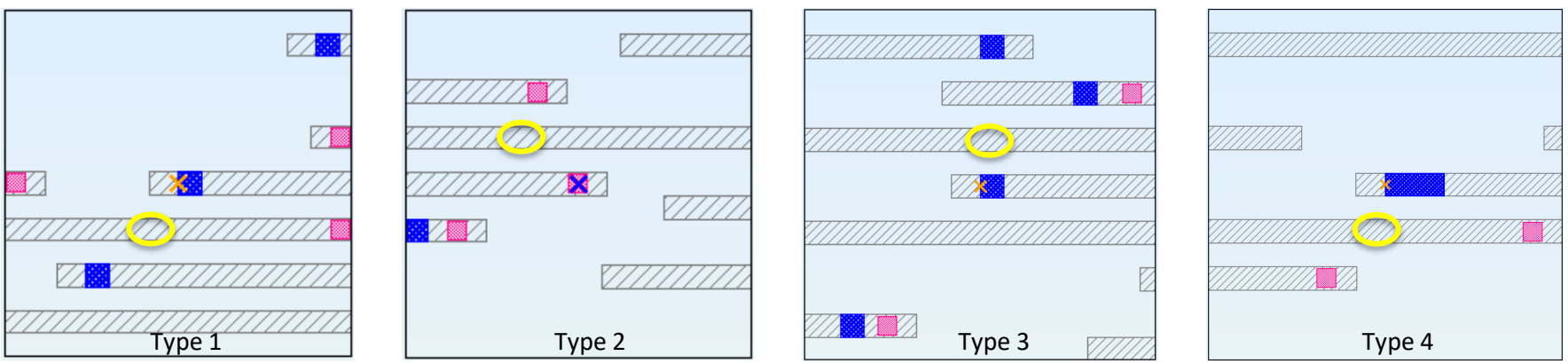
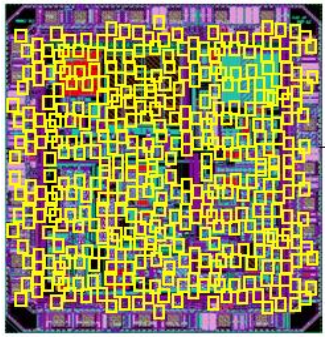


AEI Image Defect Center
Pattern Rule Center in PreOPC design
Image Defect Center in design

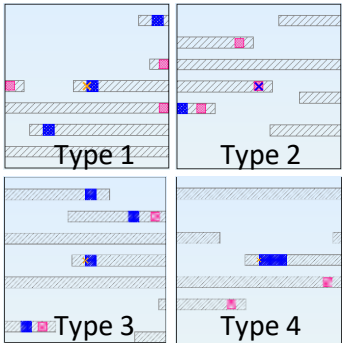
$Metal_n$
Via_{n-1}
Via_n

PCYM – Full Chip Decomposition

- Multiple layer design interaction around the defect is captured in pattern rules that is used for full chip design decomposition
- Key design vectors around the defect location are extracted and stored with related pattern information



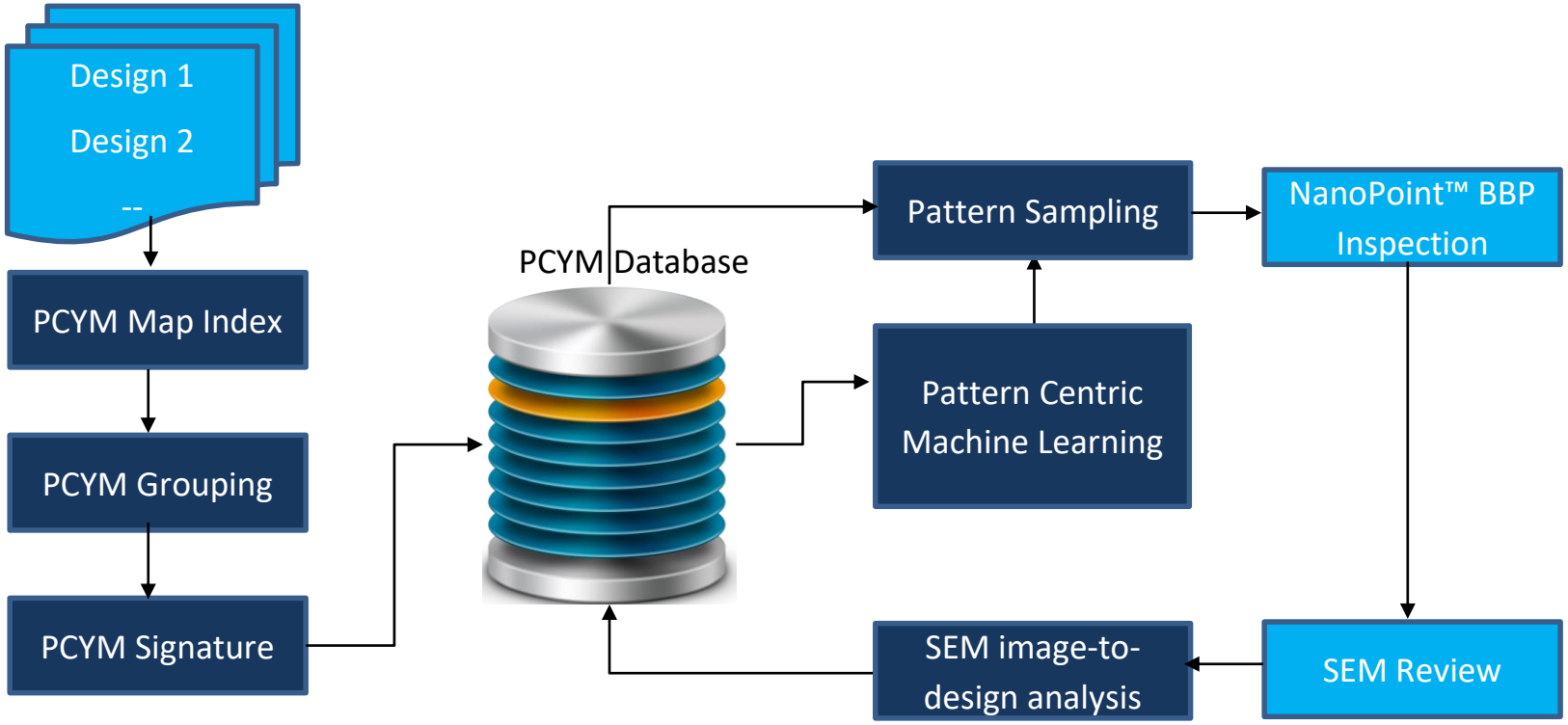
Full Chip Design



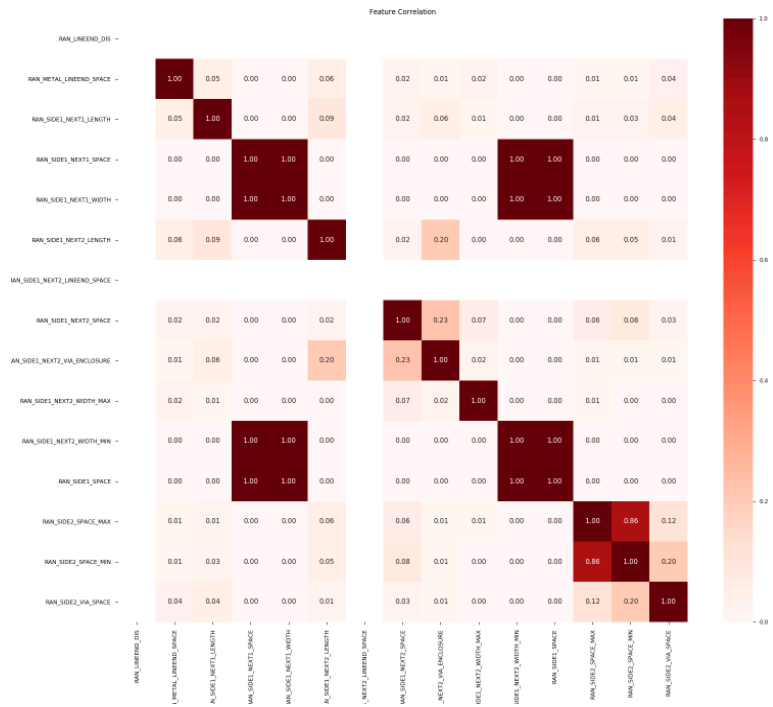
Decomposition using pattern rules

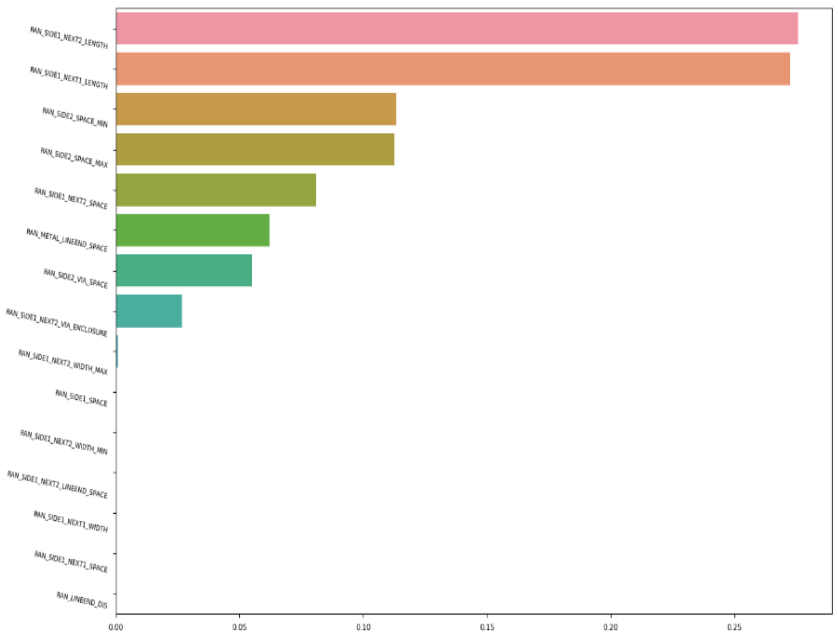
PCYM Database

Application Flow



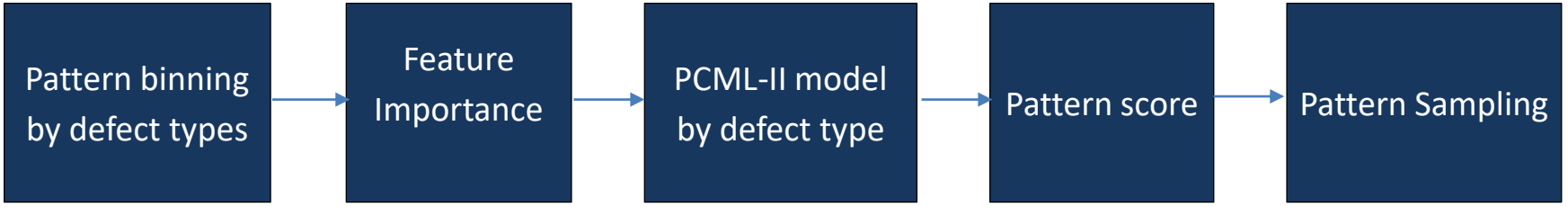
PCML-I: Rank the design vectors





- Design vector correlation matrix reveal only 2 vectors redundant
- PCML-I is used to rank the design vectors by importance for each pattern type

PCML-II: Rank the patterns



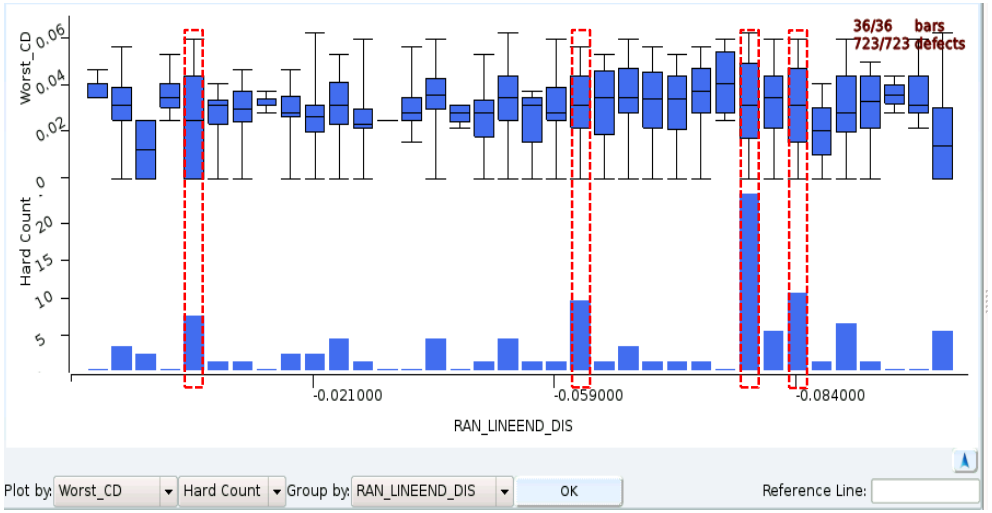
Pattern Type	Count of Signature combination	Count sampled for inspection	Count SEM Reviewed	Sites measured in the SEM images	Sites measured had Pinch defect
Type 1	1026169	29452	4854	70404	15137
Type 2	51259	17203		6155	615
Type 3	46588	16400		4085	855
Type 4	84039	30104		4991	353

- ML model is built for each pattern type
- Pattern scoring is done for each pattern type
- Final SEM review sampling is limited by the tool budget allocation

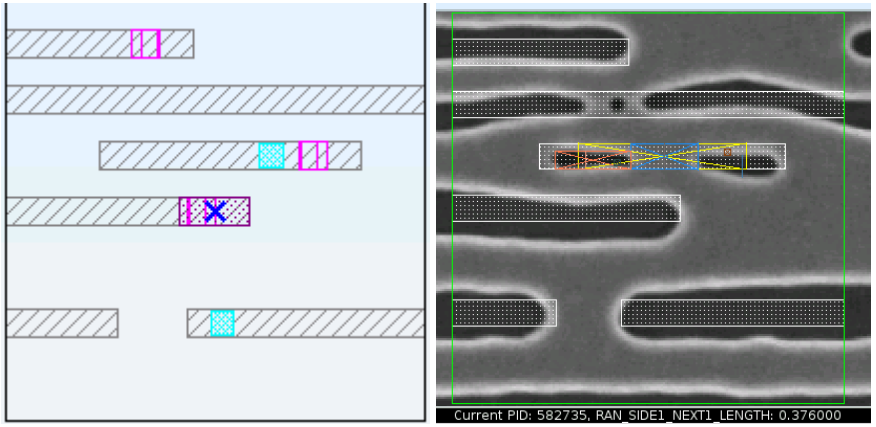
PCML-III: Image based full chip pattern ranking

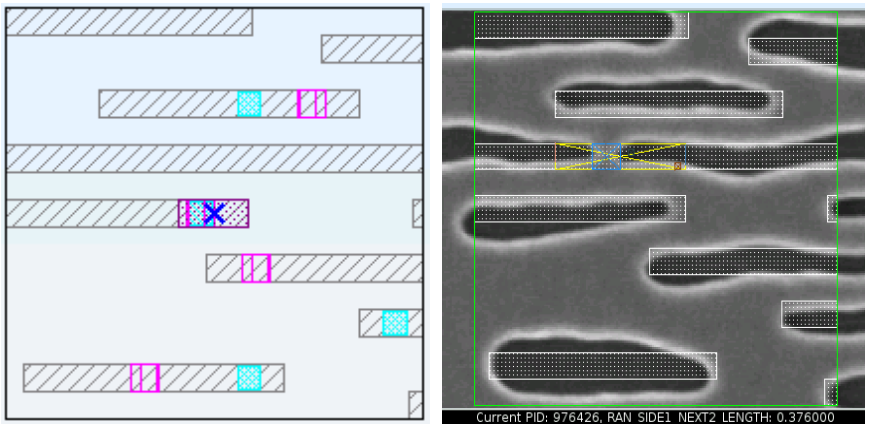
Review SEM images → Measurement of vectors in images → PCML-III model → Pattern score → Pattern Sampling

- Same vectors are measured on SEM images
- Variation on wafer is captured by the Box Plot
- Large vector variation correlates with high count of hard defects
- PCML-III model calibration from all SEM image and design data
- PCML-III utilized to rank unseen patterns in PCYM Database



Found new weak patterns





- PCML-III prediction of new weak patterns guided care area generation for discovery
- After wafer inspection and standard SEM review found more confirmed weak patterns

$Metal_n$
Via_{n-1}
Via_n

Conclusions

✓PCYM allows translation of multiple layer interaction to build full chip pattern database. It helps to track defects by associated pattern.

✓PCML-I: determined the importance of design vectors by defect type

✓PCML-II: utilized design vectors to build model by defect type and rank patterns with high purity

✓PCML-III: comprehensive SEM image measurement for the same design vectors help to correlate with wafer defect occurrence and ranked rest of the patterns in PCYM DB

✓ Identified new weak patterns

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Thank you