A comprehensive study of alignment, overlay and leveling in throughput effect under PEP-align for high volume manufacturing fab immersion group

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Outline

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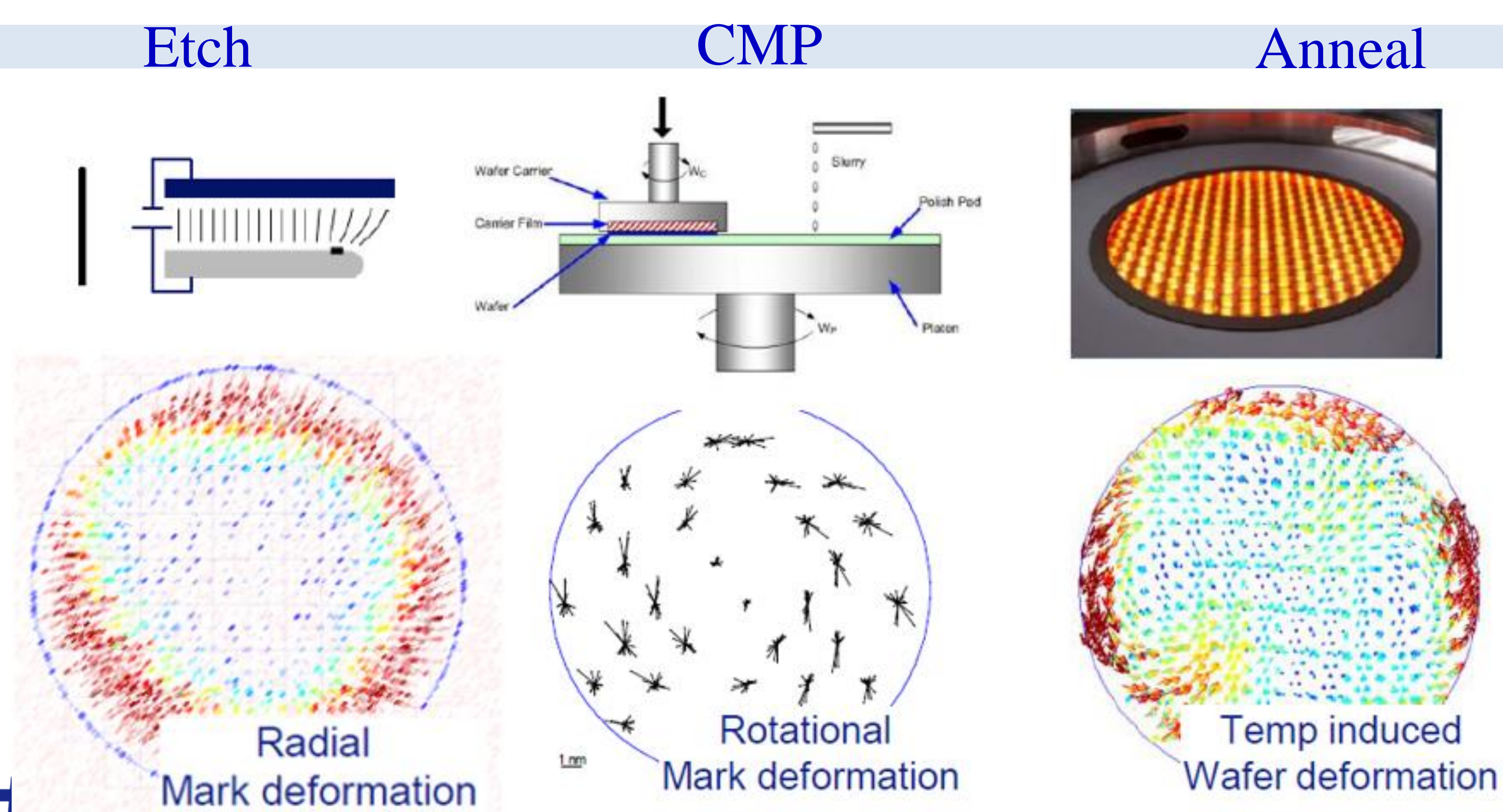
Introduction

Current challenge: overlay suffers from higher order wafer/mark deformation

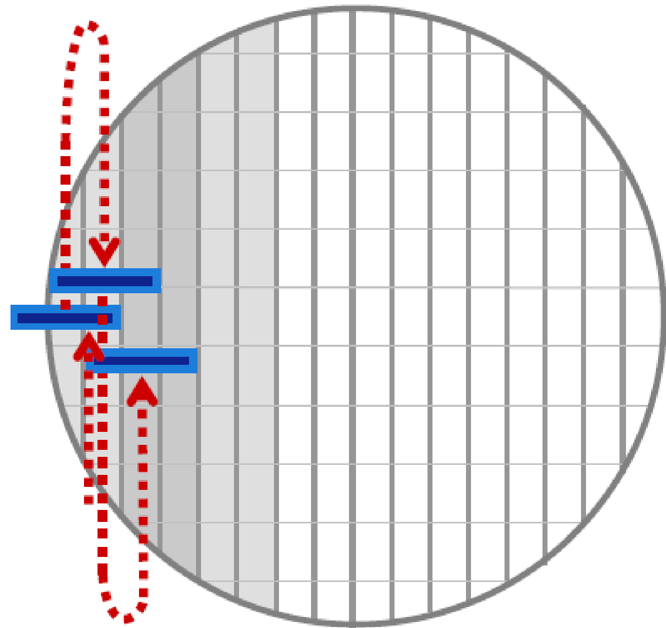
- Current lithography process suffer big overlay challenge due to Etch, CMP, Anneal.et al. process induce wafer/mark have higher order deformation, wafer to wafer behavior also may different. Linear alignment model (6pa) are insufficient to capture these effects.
- High order alignment model is needed, but need more alignment mark, throughput suffer big challenge, PEP-align option is induced to solved this challenge.



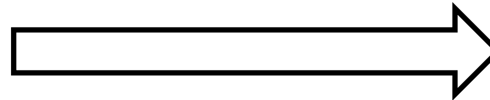
Layout independent Leveling(LIL) introduction

Layout Dependent Leveling(LDL)

Stroke routing follows layout, wafer map measured in ≥11 strokes for full wafer coverage

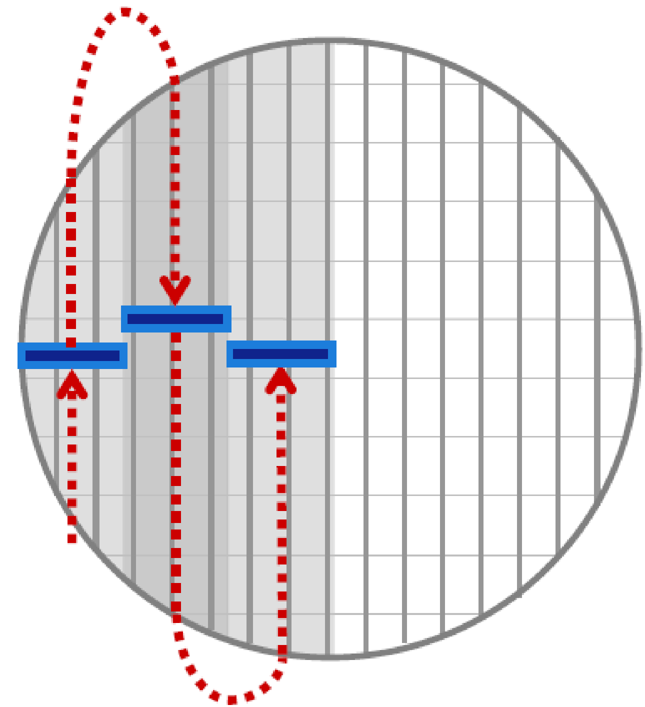


Wafer Z Map time gain by fewer Level Sensor strokes



Layout Independent Leveling(LIL)

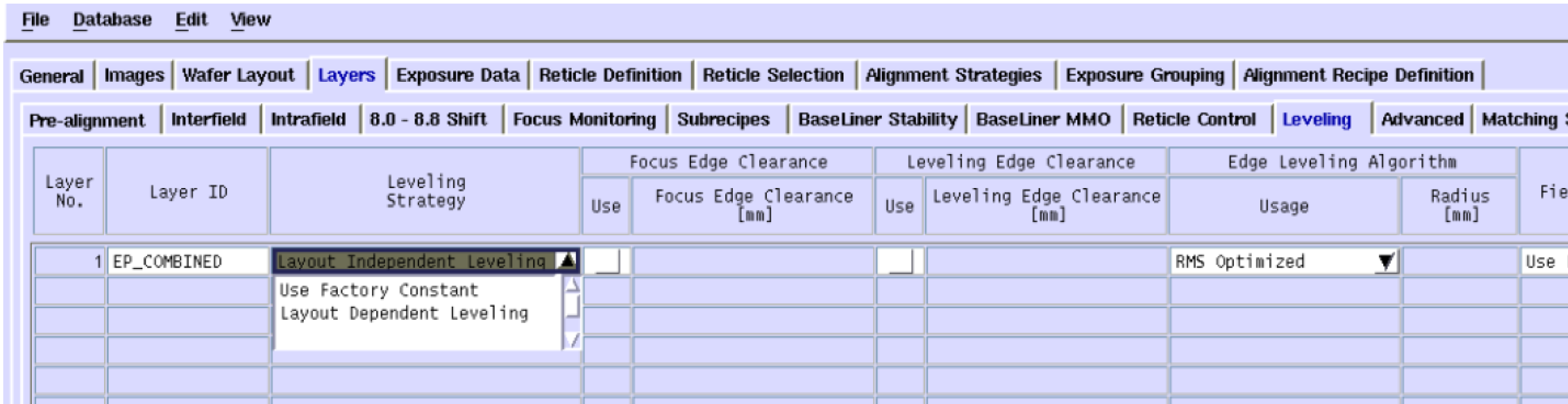
Fixed routing, wafer map always measured in **6 strokes**



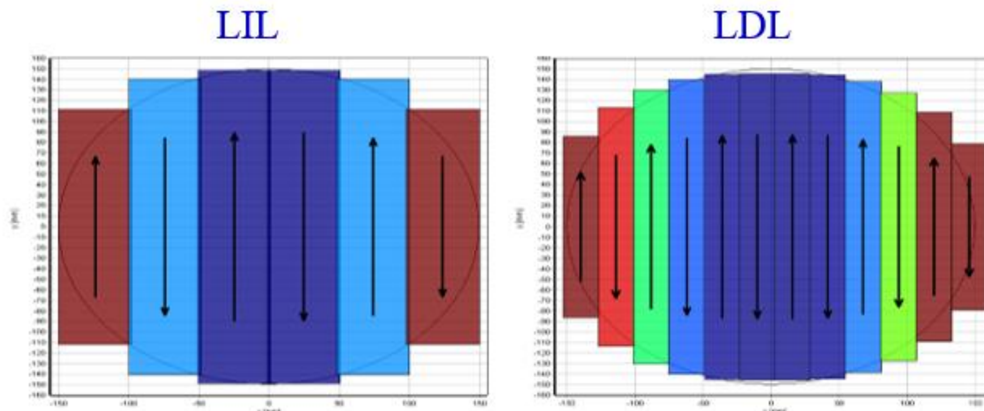
Experiment Result

Layout Independent Leveling(LIL) option enable and verify

- When Layout Independent Leveling(LIL) license installed, customer can enable the option by recipe setting: (RDM→ Layers→ Leveling→ Leveling Strategy)

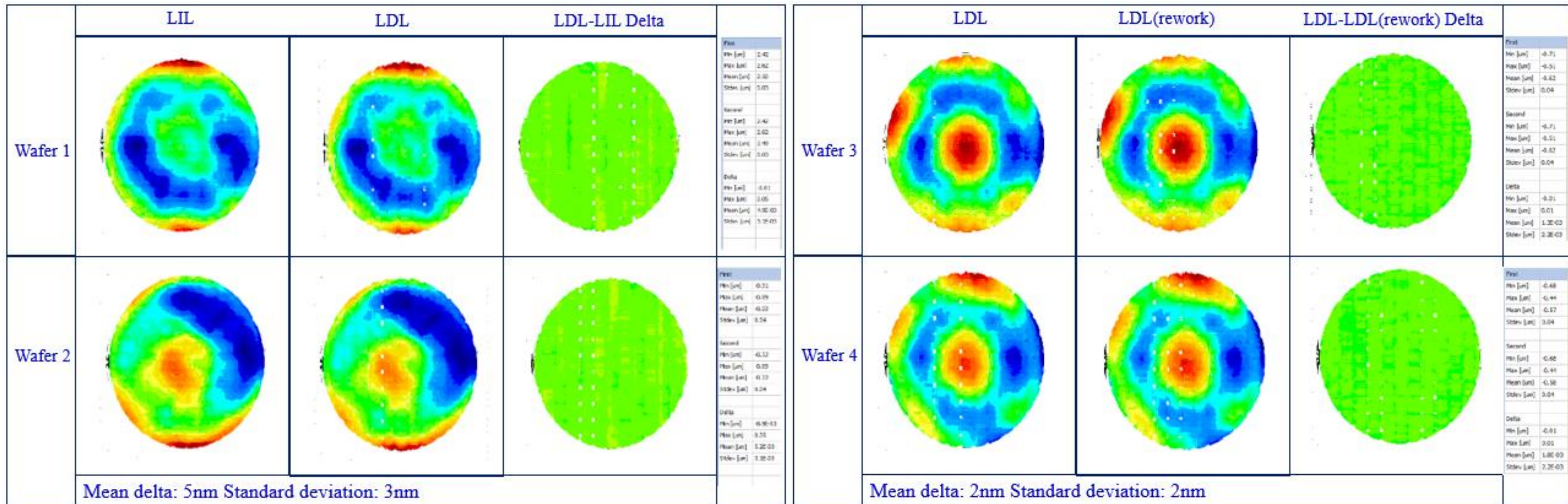


- When Layout Independent Leveling(LIL) option enable, collect MDL use FLAT 7.4 to verify function if work



Layout Independent Leveling(LIL) and Layout Dependent Leveling(LDL) leveling height map compare

Condition	Layer	Process wafer	Leveling strategy	Condition	Layer	Process wafer	Leveling strategy	Delta
1	Layer A	2	LIL	2	Layer A	2	LDL	LIL-LDL
3	Layer A	2	LDL	4	Layer A	2	LDL(rework)	LDL-LDL(rework)

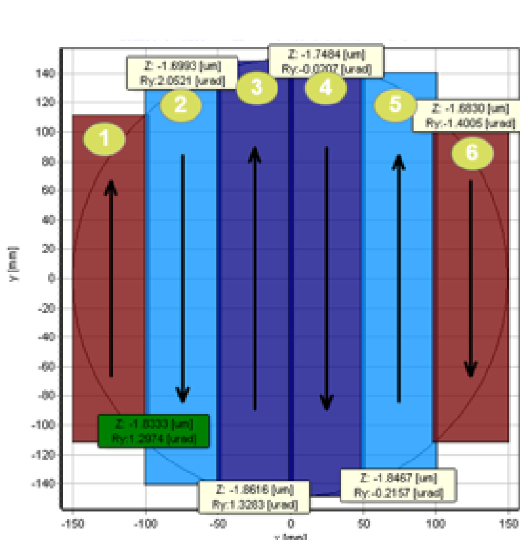


Layout Independent Leveling(LIL) throughput evaluation

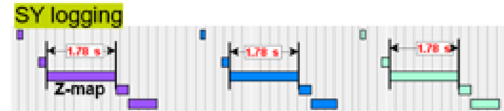
Condition	Layer	Process wafer	Leveling strategy	Stroke count	Wafer Z Map time(s)	FIWA mark count	FIWA time(s)
1	Layer B	1	LIL	6	1.78S	/	/
2	Layer B	1	LDL	12	3.36S	28 pairs	4.40

LIL lot Z-map

Only scan 6 strokes which takes 1.78s for Z-map



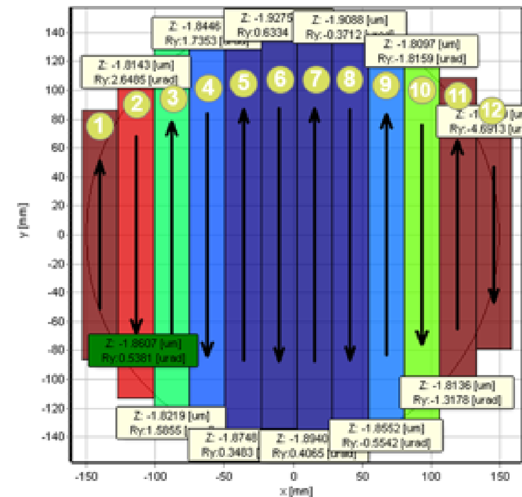
SY logging



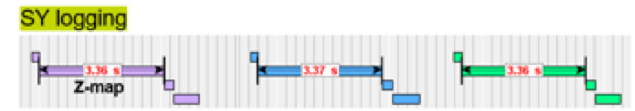
Stroke	PREP(s)	SCAN(s)
1	0.1876	0.115
2	0.1188	0.192
3	0.097	0.23
4	0.0912	0.23
5	0.097	0.192
6	0.1188	0.115
Total	1.78	

LDL lot Z-map

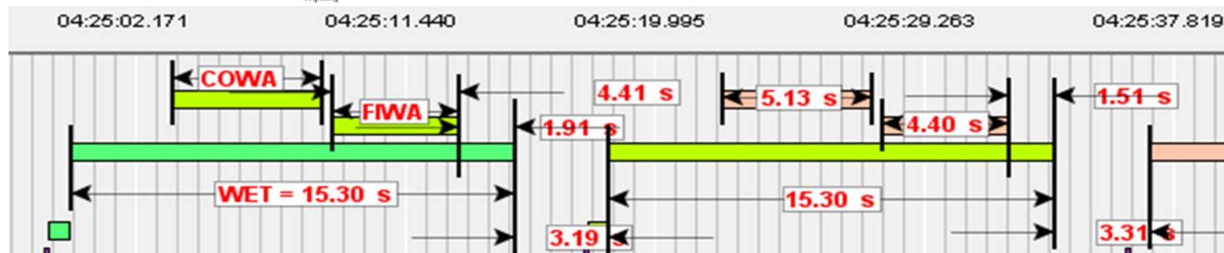
Scan 12 strokes which takes 3.36s for Z-map



SY logging



Stroke	PREP(s)	SCAN(s)
1	0.1762	0.0864
2	0.1466	0.118
3	0.1242	0.1576
4	0.1094	0.1904
5	0.1	0.2114
6	0.0962	0.2144
7	0.0958	0.2144
8	0.0966	0.2086
9	0.1014	0.1844
10	0.112	0.1502
11	0.128	0.1096
12	0.1526	0.079
Total	3.36	



Layout Independent Leveling(LIL) alignment performance evaluation

a. 6P 15 A mark		ROPI mean X 4.2nm Y 4.8nm
b. HOWA3 30 A mark		ROPI mean X 1.2nm Y 2.5nm
c. RBF 45 A mark		ROPI mean X 0.75nm Y 1.25nm

Condition	Layer	Mark type	Mark count	Model
1	Layer C	A mark	15	6P
2	Layer C	A mark	30	HOWA3
3	Layer C	A mark	45	RBF

Conclusion

Conclusion

- LIL leveling strategy and LDL leveling strategy LS obtain wafer surface height map is comparable, dose not significantly impact the focus performance on wafer.

- LIL leveling strategy Wafer Z Map time is shorter about 1.58S (12 strokes production for reference) than LDL leveling strategy Wafer Z Map time, more strokes count can gain more Wafer Z Map time saved.

- Under the condition of throughput keep, LIL leveling strategy can tolerate the placement of more FIWA marks, more FIWA marks can use higher order model, can improve HVM overlay stability.

Thanks

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