

A comprehensive study of alignment, overlay and leveling in throughput effect under PEP-align for high volume manufacturing fab immersion group

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Outline

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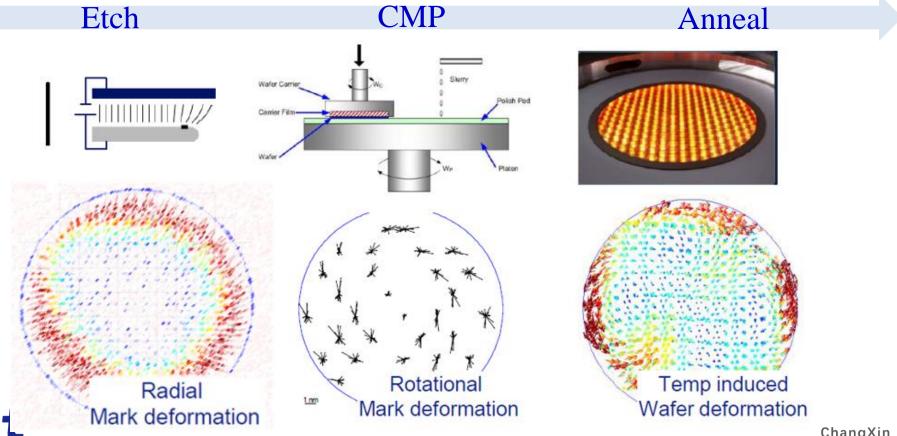


Introduction



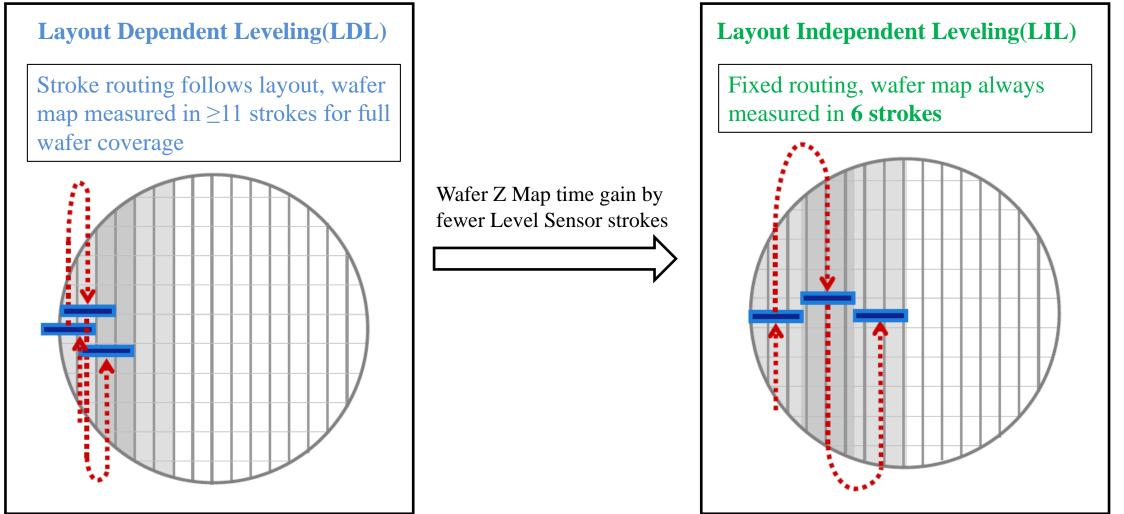
Current challenge: overlay suffers from higher order wafer/mark deformation

- Current lithography process suffer big overlay challenge due to Etch, CMP, Anneal.et al. process induce wafer/mark have higher order deformation, wafer to wafer behavior also may different. Linear alignment model (6pa) are insufficient to capture these effects.
- High order alignment model is needed, but need more alignment mark, throughput suffer big challenge, PEP-align option is induced to solved this challenge.



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Layout independent Leveling(LIL) introduction





Experiment Result

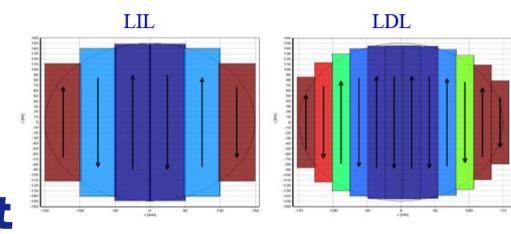


Layout Independent Leveling(LIL) option enable and verify

 When Layout Independent Leveling(LIL) license installed, customer can enable the option by recipe setting: (RDM→ Layers→ Leveling→ Leveling Strategy)

E	<u>File Database Edit View</u>									
G	General Images Wafer Layout Layers Exposure Data Reticle Definition Reticle Selection Alignment Strategies Exposure Grouping Alignment Recipe Definition									
l	Pre-align	ment Interfield	Intrafield 8.0 - 8.8 Shift Focus N	Ionito	ring Subrecipes BaseLine	r Stal	bility BaseLiner MMO Reti	cle Control Leveling A	dvanced Mat	tching {
					Focus Edge Clearance	Le	eveling Edge Clearance	Edge Leveling Alg	gorithm	
	Layer No.	Layer ID	Leveling Strategy	Use	Focus Edge Clearance [mm]	Use	Leveling Edge Clearance [mm]	Usage	Radius [mm]	Fie
[1	EP_COMBINED	Layout Independent Leveling 🔺					RMS Optimized 🛛 🔻	1	Use I
			Use Factory Constant Layout Dependent Leveling							

• When Layout Independent Leveling(LIL) option enable, collect MDL use FLAT 7.4 to verify function if work



Layout Independent Leveling(LIL) and Layout Dependent Leveling(LDL) leveling height map compare

Condition	Layer	Process wafer	Leveling strategy	Condition	Layer	Process wafer	Leveling strategy	Delta
1	Layer A	2	LIL	2	Layer A	2	LDL	LIL-LDL
3	Layer A	2	LDL	4	Layer A	2	LDL(rework)	LDL-LDL(rework)

	LIL	LDL	LDL-LIL Delta			LDL	LDL(rework)	LDL-LDL(rework) Delta	
Wafer 1				Plane Proj 2.42 Proj (erg) 2.40 Proj Proj (erg) 2.00 State (erg) 2.00 State (erg) 2.00 State (erg) 2.00 Proj (erg) 2.00 State (erg) 2.00 Proj (erg) 2.40 Proj (erg) 2.40 Proj (erg) 2.40 Proj (erg) 2.40 Proj (erg) 2.40 Proj (erg) 2.40 Proj (erg) 1.00 State (erg) 2.00 State (erg) 0.01 Proj (erg) 3.26.00 Proj (erg) 3.26.00 Tobin (erg) 3.26.00	Wafer 3				Real -0.71 Mo (µm) -0.71 Max (µm) -0.51 Max (µm) -0.51 Max (µm) -0.22 Stever (µm) 0.04 Second
Wafer 2				Part	Wafer 4				Proc
	Mean delta: 5nm Standard	d deviation: 3nm				Mean delta: 2nm Standa	ard deviation: 2nm		



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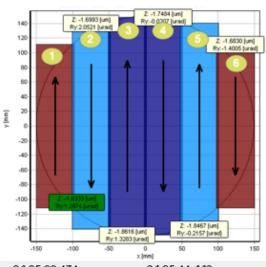
Layout Independent Leveling(LIL) throughput evaluation

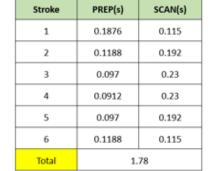
Condition	Layer	Process wafer	Leveling strategy	Stroke count	Wafer Z Map time(s)	FIWA mark count	FIWA time(s)
1	Layer B	1	LIL	6	1.785	/	/
2	Layer B	1	LDL	12	3.368	28 pairs	4.40

LDL lot Z-map

LIL lot Z-map

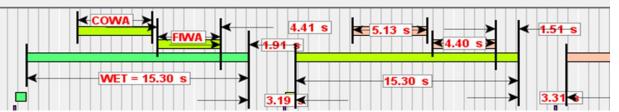
Only scan 6 strokes which takes 1.78s for Z-map





04:25:02.171 04:25:11.440 04:25:29.263

04:25:37.819



04:25:19.995

GXMt

Z: -1.9275 Z: -1.9088 [un] Ry:0.6334 Ry:-0.3712 Z: -1.8446 Ry:1.7353 [s 1.4 Z: -1.8097 [um] Ry:-1.8159 [urad] 120 Z: -1.0143 [un] Ry:2.6485 [ured] Ry:-4.6913 Jurad -100 Z: -1.8136 [um] Ry.-1.3178 [urad] -120 Z: -1.8219 [um] Ry:1.5055 [r Z: -1.8552 [un] -140 Z: -1.8748 Z: -1.8940 Ry:-0.5542 [urad] Ry:0.3483 Ry:0.4065 [urad] 150 -150 -100 -50 50 100 \times [mm]

Scan 12 strokes which takes 3.36s for Z-map



Stroke	PREP(s)	SCAN(s)
1	0.1762	0.0864
2	0.1466	0.118
3	0.1242	0.1576
4	0.1094	0.1904
5	0.1	0.2114
6	0.0962	0.2144
7	0.0958	0.2144
8	0.0966	0.2086
9	0.1014	0.1844
10	0.112	0.1502
11	0.128	0.1096
12	0.1526	0.079
Total	3.	36

Layout Independent Leveling(LIL) alignment performance evaluation

	59 F_PoK1_X 56 F_PoK1_Y		Condition	Laye
	6.4 6.2 5	ROPI mean	1	Layer
a. 6P 15 A mark		X 4.2nm 2		Layer
	4 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Y 4.8nm	Layer	
b. HOWA3 30 A mark		ROPI mean X 1.2nm Y 2.5nm		
c. RBF 45 A mark		ROPI mean X 0.75nm Y 1.25nm		

Condition	Layer	Mark type	Mark count	Model
1	Layer C	A mark	15	6P
2	Layer C	A mark	30	HOWA3
3	Layer C	A mark	45	RBF



Conclusion



Conclusion

- LIL leveling strategy and LDL leveling strategy LS obtain wafer surface height map is comparable, dose not significantly impact the focus performance on wafer.
- LIL leveling strategy Wafer Z Map time is shorter about 1.58S (12 strokes production for reference) than LDL leveling strategy Wafer Z Map time, more strokes count can gain more Wafer Z Map time saved.
- Under the condition of throughput keep, LIL leveling strategy can tolerate the placement of more FIWA marks, more FIWA marks can use higher order model, can improve HVM overlay stability.



Thanks



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