A Study of the Advantages to the Photolithography Process brought by the High NA EUV Exposure Tool in Advanced Logic Design Rules

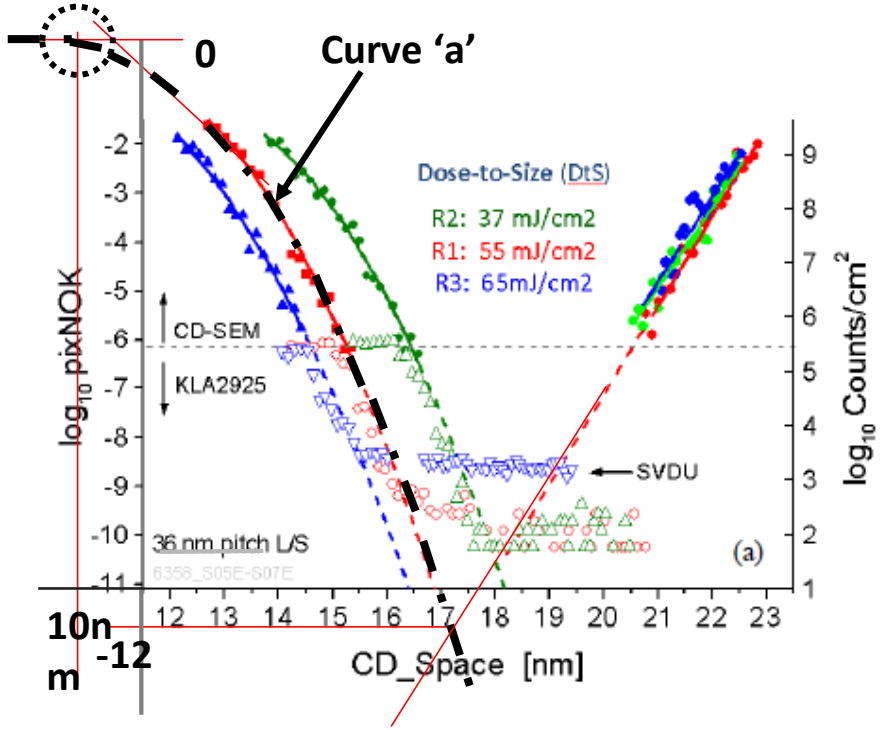
❖ Yanli Li*, Xiaona Zhu, Shaofeng Yu, and Qiang Wu*

Outline

- **Background**
- **Typical Metal Layer Design Rules in High NA EUV Lithography**
  - Metal Layer TtT Design Rule
  - 90° Bend Design Rule
  - Minimum area Design Rule
- **A SRAM Layout of 3 nm CFET**
- **A 45° local interconnect exposed under High NA EUV Lithography**
- **Summary**

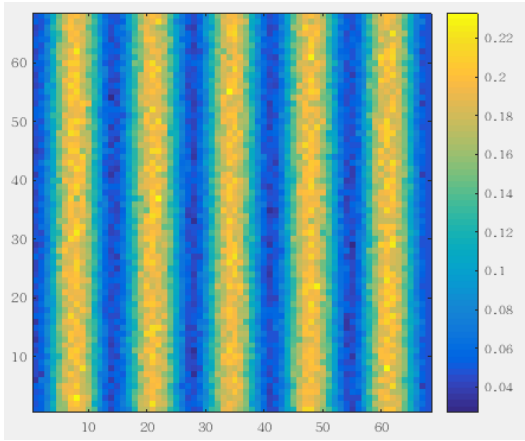
Background

Defectivity model and IMEC wafer data*

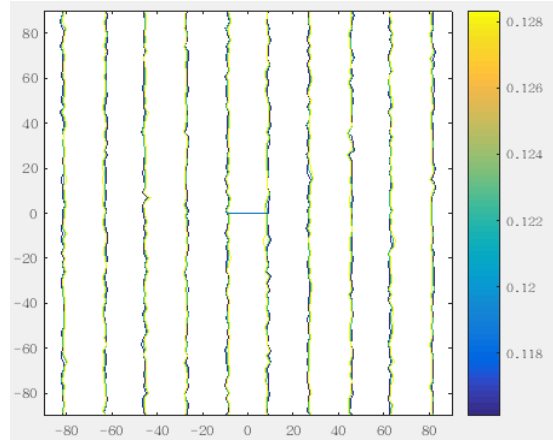


- IMEC wafer data: Unbiased LWR ~2.7 nm.
- Defect density~10^{-12}, pitch 36 nm.

0.33 NA Simulation Data



Aerial image with stochastics



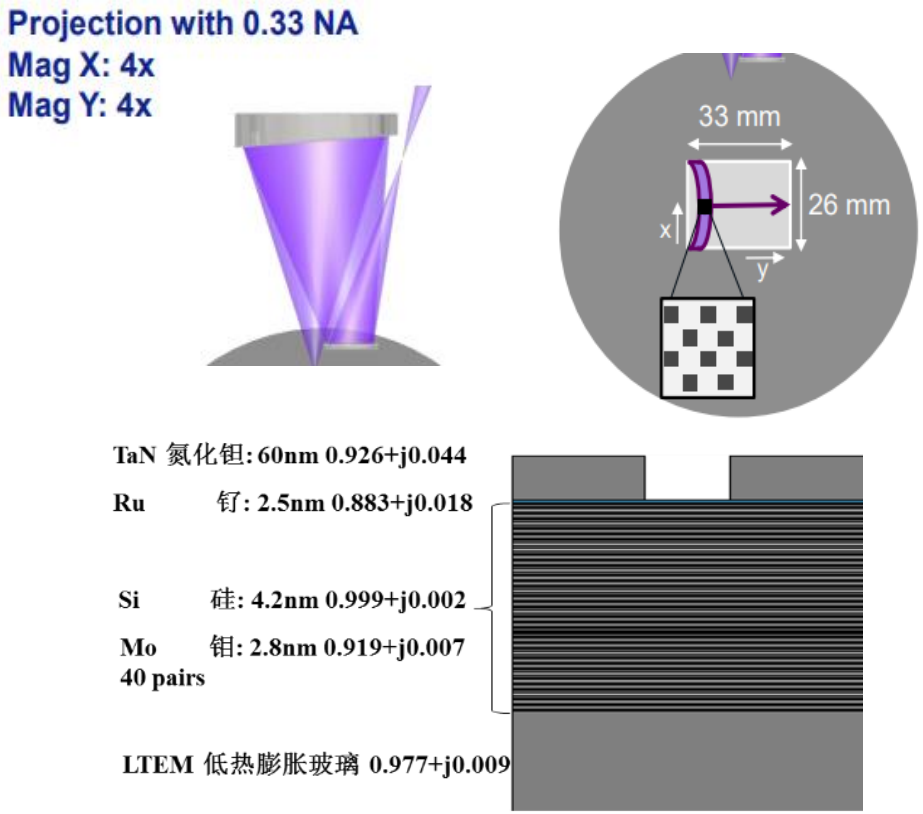
Contour with stochastics

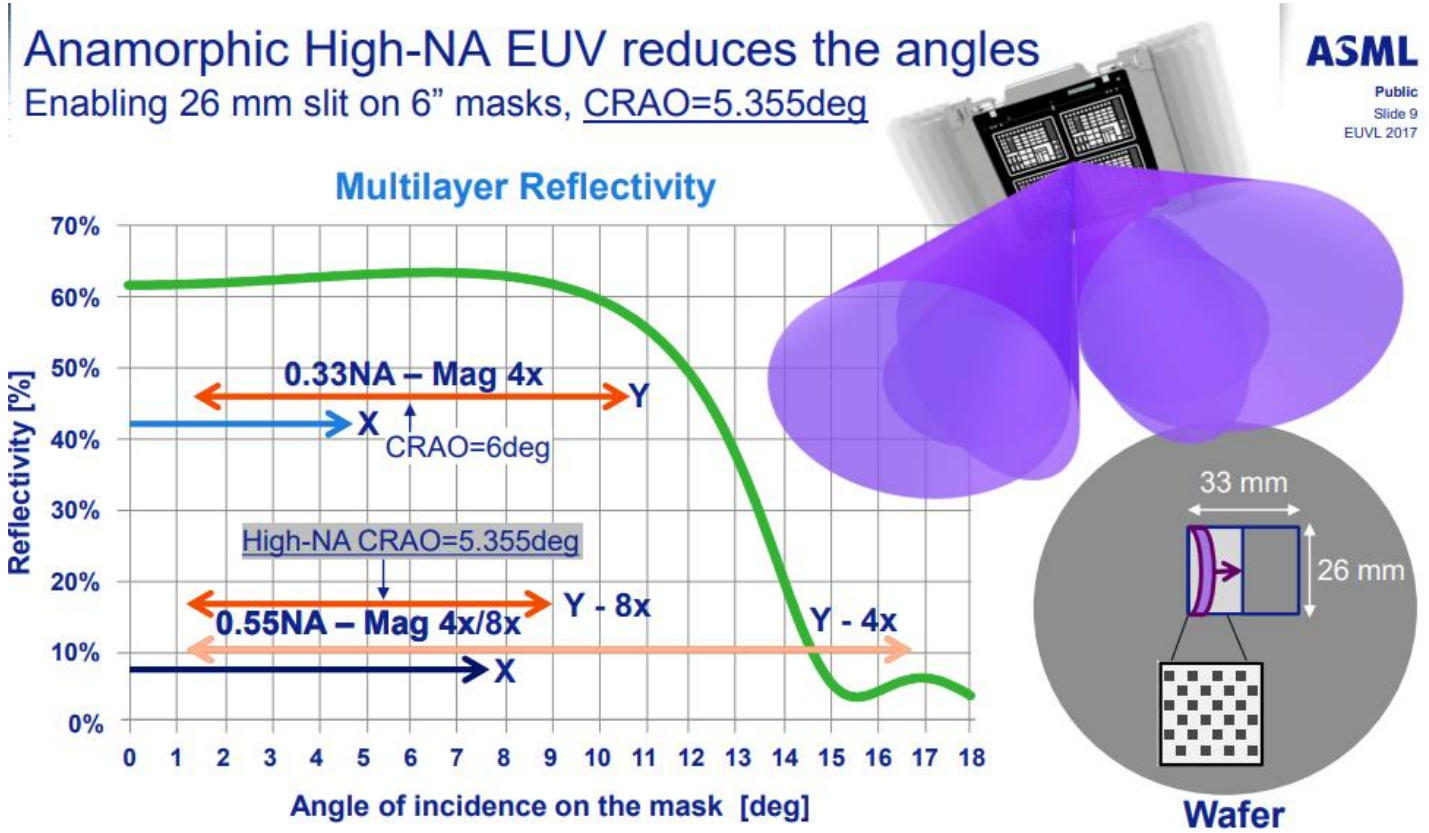
- Pitch 36 nm, CD~18 nm, Energy=55mJ/cm^2.
- Simulation unbiased LWR~2.67 nm.
- EL ~ 19% > 18% .
- Illumination: QC35° 0.9/0.7, 0.33 NA, PR thickness: 30 nm.

* Yanli Li"A Simulation Study for Typical Design Rule Patterns and Stochastic Printing Failures in a 5 nm Logic Process with EUV Lithography", IEEE Xplore, 2020.

Background

- 40 pairs Mo/Si high reflection layers, TaN absorber layer and Ru protection layer.
- The Chief Ray Angle at Object space (CRAO) of incidence in 0.55 NA EUV lithography is 5.355°.
- 0.33 NA-Mag: 4x-X/Y; 0.55 NA-Mag: 4x-X, 8x-Y .





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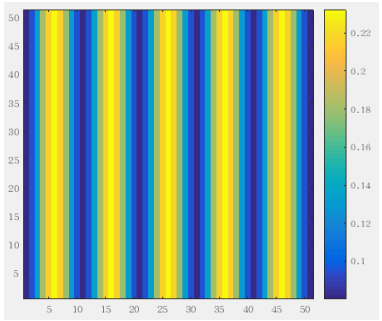
* https://www.researchgate.net/publication/320438600; "High-NA EUV lithography enabling Moore's law in the next decade".

Background

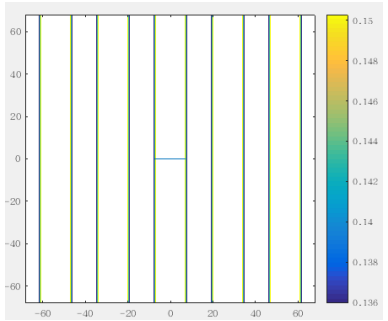
Typical dimensions for metal layers under several advanced logic nodes*

Logic Tech Node	3 nm	2 nm	1.5 nm	1 nm
Metal pitch（nm）	20~26	14~18	14	14
Lithography process	0.33 NA EUV SALE2	0.55 NA EUV SALE2	0.55 NA EUV SALE2	0.55 NA EUV SALE2

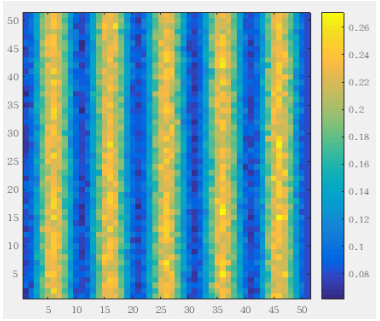
0.55 NA EUV Simulation Data



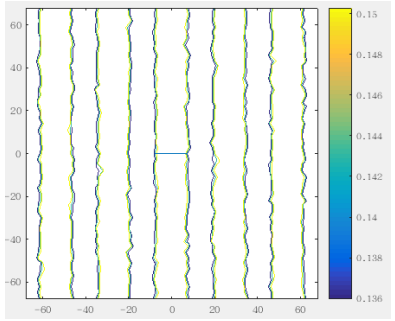
Aerial image



Contour



Aerial image with stochastics

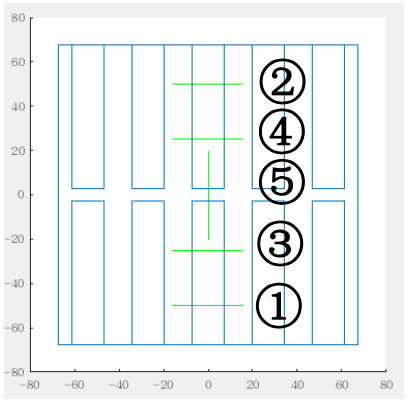


Contour with stochastics

- Pitch 28 nm, CD~15 nm, EL ~ 18.5% > 18% .
- Unbiased LWR~2.2 nm, Energy~55mJ/cm^2.
- Illumination: Quasar 35° 0.7/0.5, 0.55 NA, PR thickness: 30 nm.

*中国集成电路技术发展路线图 2019——国家集成电路创新中心.

Metal Layer TtT Design Rule in High NA EUV



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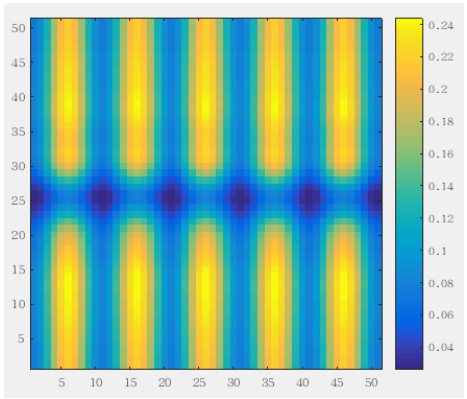

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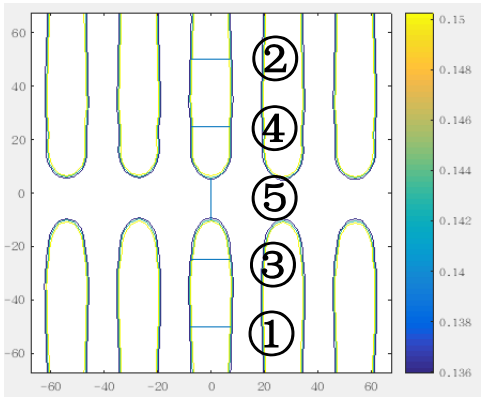
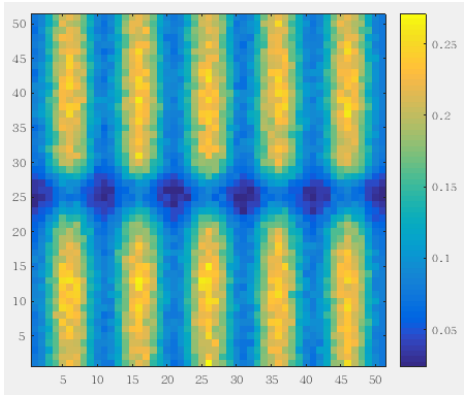
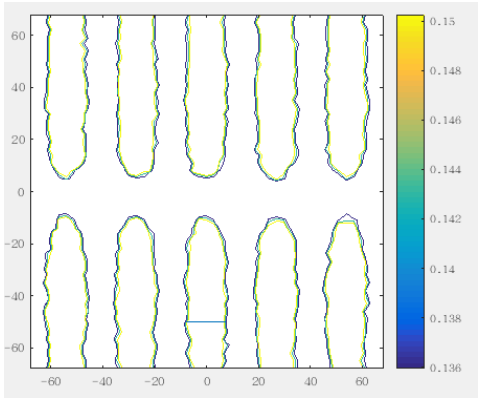


Contour

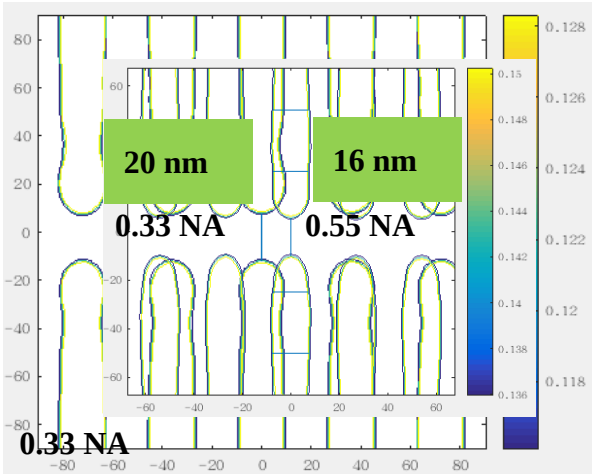
Line cut	①	②	③
EL	18.5%	18.0%	17.5%
CD (nm)	15	15	14.3
Line cut	④	⑤	
EL	17.4%	13.3%	
CD (nm)	14.3	15.7	



Aerial image with stochastics



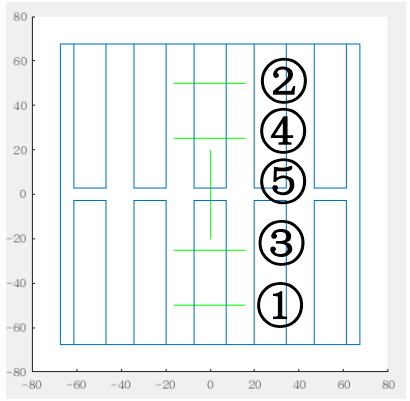
Contour with stochastics



- ① is dense pattern, EL must be ≥ 18%; the TtT EL must be ≥ 13%* both in 0.33 and 0.55 NA EUV.
- 0.55 NA EUV, the TtT minimum CD is ~16 nm; 0.33 NA EUV, the corresponding minimum CD is 20 nm*.
- 0.33-0.55 NA, 1D CD 18-15 nm, therefore, the TtT CD reduction of 20% is reasonable.

* Yanli Li"A Simulation Study for Typical Design Rule Patterns and Stochastic Printing Failures in a 5 nm Logic Process with EUV Lithography", IEEE Xplore, 2020.

The simulation results from Quasar 35° and SO source



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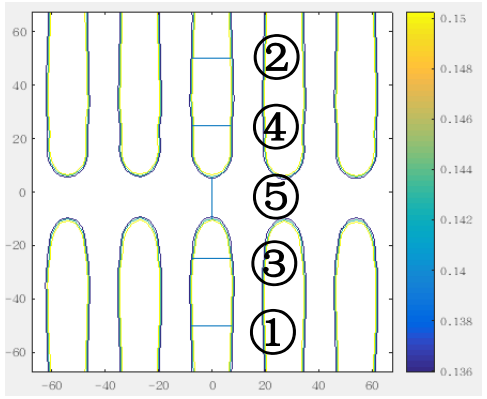
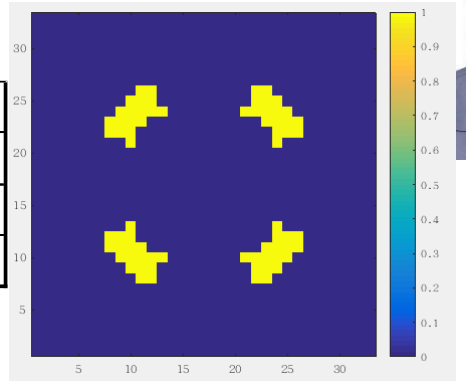
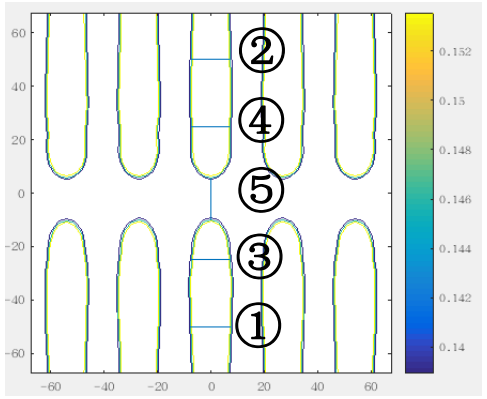


Contour

Quasar 35° 0.7/0.5					
Line cut	①	②	③	④	⑤
EL	18.5%	18.0%	17.5%	17.4%	13.3%
CD (nm)	15	15	14.3	14.3	15.7

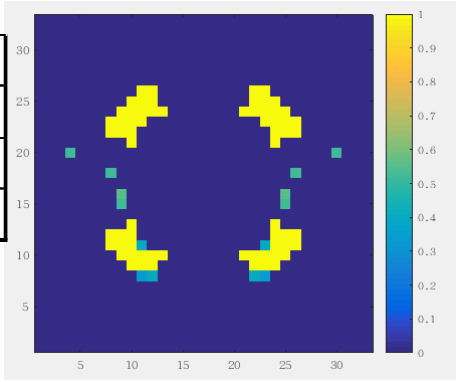


Quasar 35° 0.7/0.5



Contour

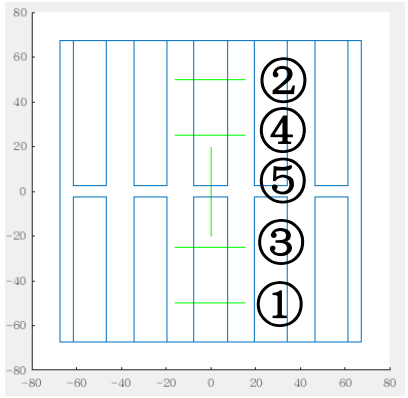
SO Source					
Line cut	①	②	③	④	⑤
EL	18.6%	18.1%	17.7%	17.6%	13.2%
CD (nm)	15	15	14.3	14.3	15.7



SO Source

- We have made a preliminary Source Optimization for this pattern.
- The simulation results show that the improvement of process window by Source Optimization is not obvious.

Metal Layer TtT Design Rule in High NA EUV



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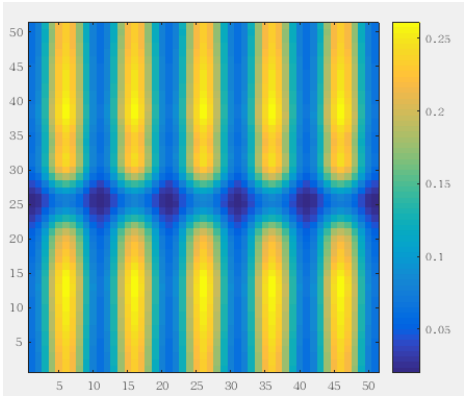
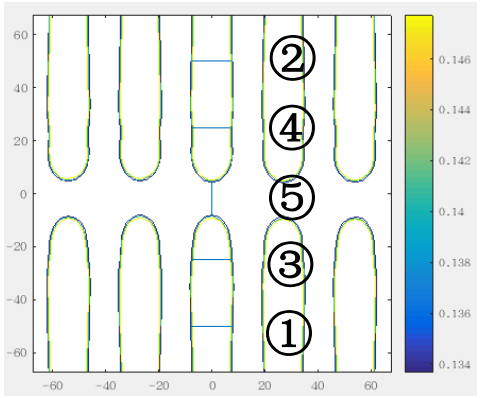
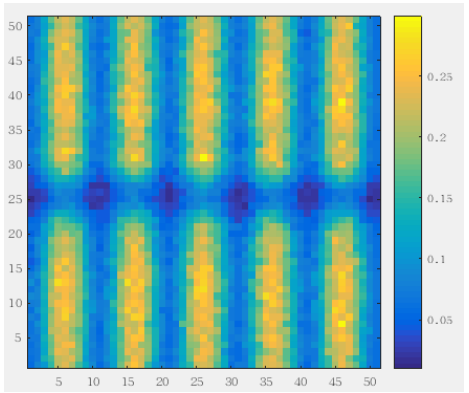


Aerial image

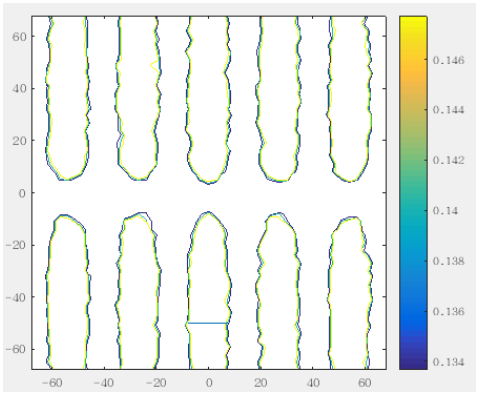


Contour

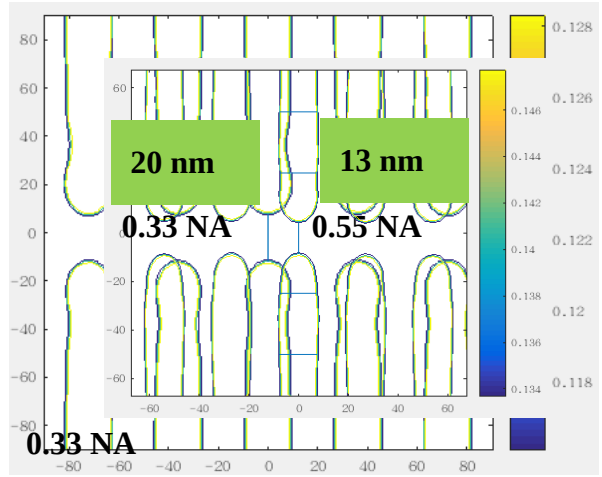
Line cut	①	②	③
EL	22.6%	21.8%	20.6%
CD (nm)	15	15	14.5
Line cut	④	⑤	
EL	20.3%	13.1%	
CD (nm)	14.5	13.3	



Aerial image with stochastics

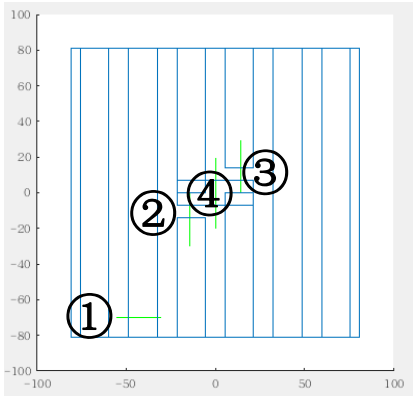


Contour with stochastics



- The TtT minimum CD is ~13.3 nm in 0.55 NA EUV .
- We need to increase the exposure energy by ~15% in order to maintain the LWR to the original level of 2.2 nm.

90° bend Design Rule in High NA EUV Lithography



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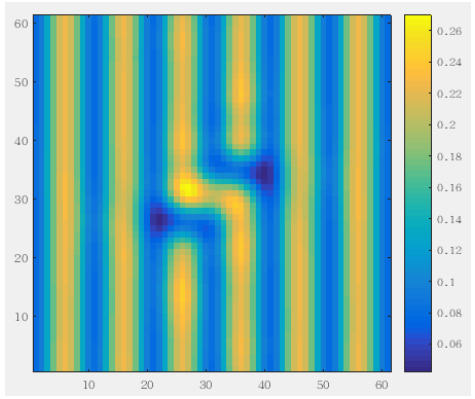

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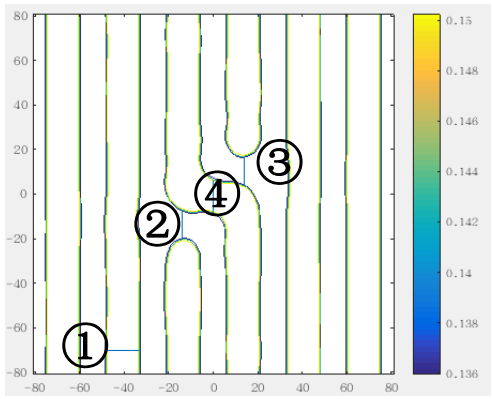
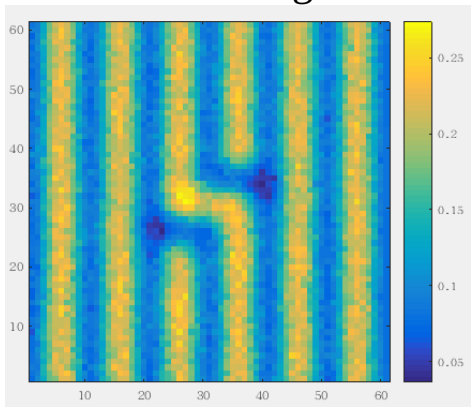
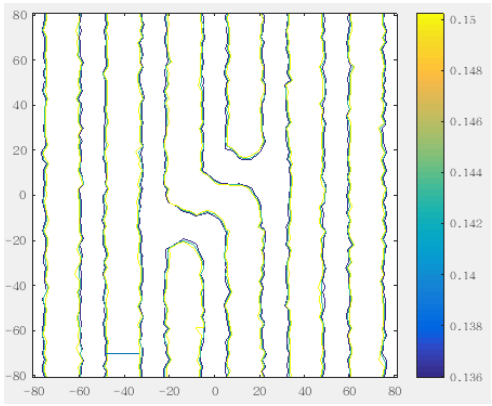


Contour

Line cut	①	②
EL	18.5%	13.5%
CD (nm)	15	13
Line cut	③	④
EL	13.6%	13.2%
CD (nm)	13	14.5



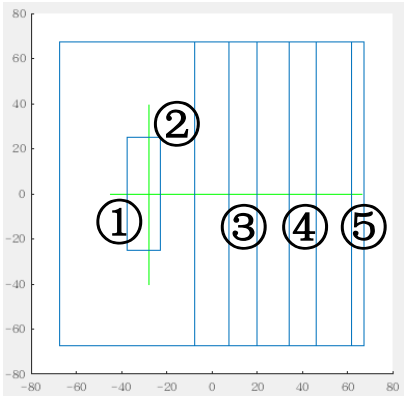
Aerial image with stochastics



Contour with stochastics

- ① is dense pattern, EL must be ≥ 18%.
- The minimum CD of tip to short line is ~13 nm in 0.55 NA EUV, and the EL is larger than 13%.
- When the anchor pitch is 28 nm, the 1.5D design rule is feasible at critical patterns and can reduce masks of metal layer.

Minimum area Design Rule in High NA EUV Lithography



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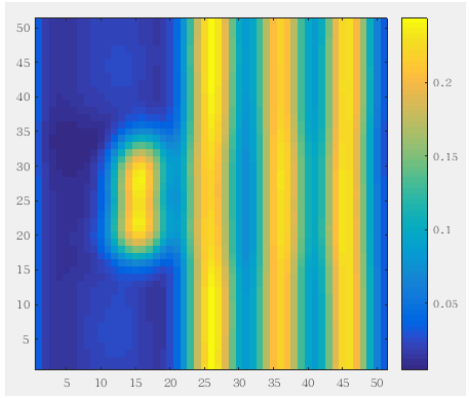

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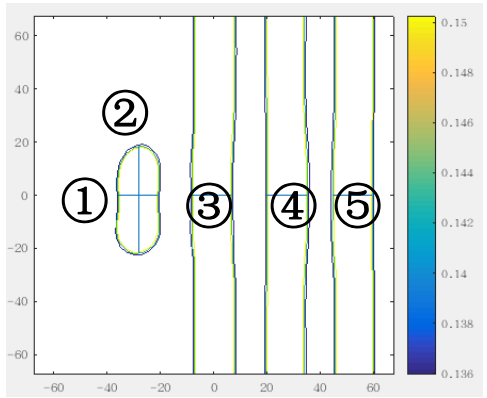
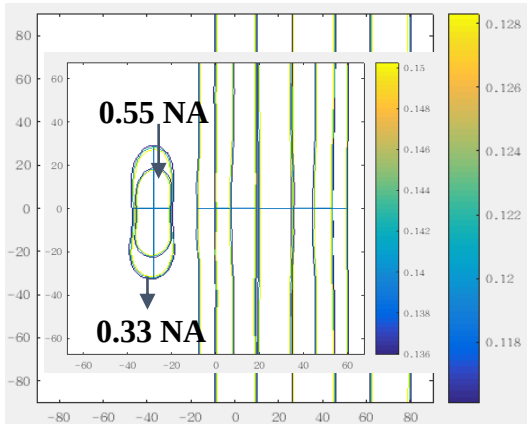
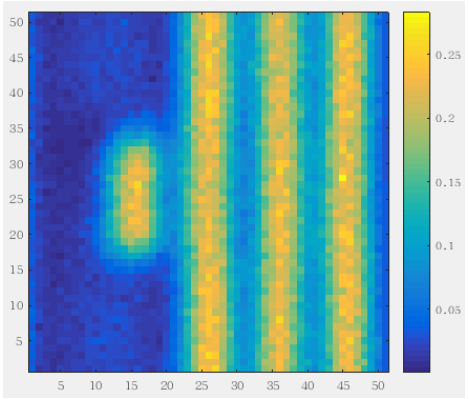


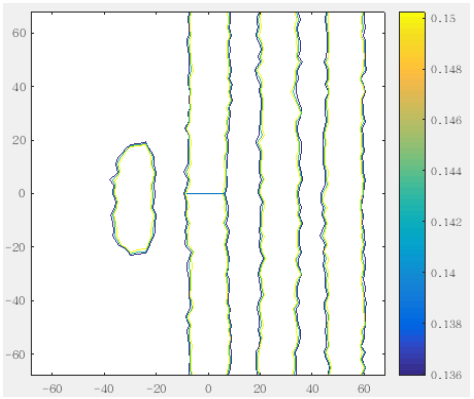
Contour



Line cut	①	②	③
EL	18.8%	30.0%	18.5%
CD (nm)	15.1	40.5	15
Line cut	④	⑤	
EL	18.0%	17.5%	
CD (nm)	15.1	14.9	



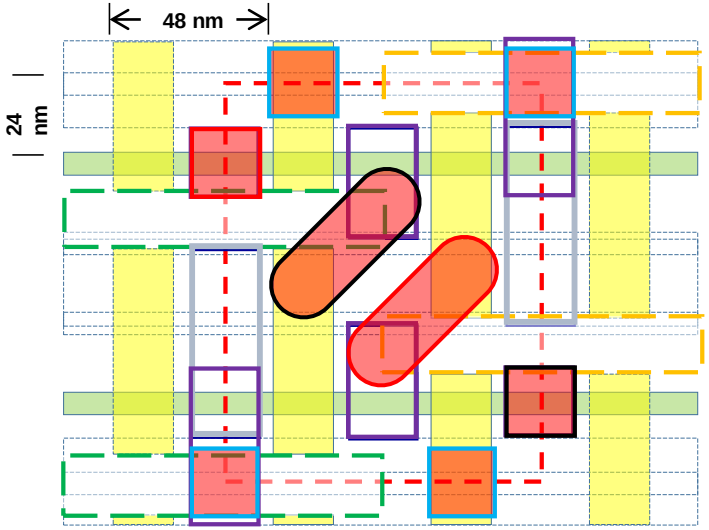
Aerial image with stochastics



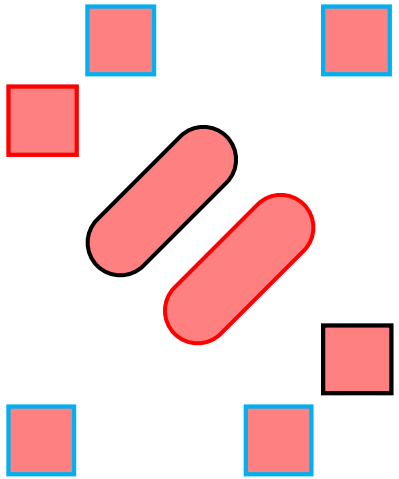
Contour with stochastics

- Line cut ① is the isolated trench, EL must be ≥ 13%.
- 0.55 NA EUV, the minimum area is ~3×15×15 nm^2 ; 0.33 NA EUV, the minimum area is 4.5~5×18×18 nm^2.
- Therefore, the minimum exposure area can be reduced by 50% in high NA EUV lithography.

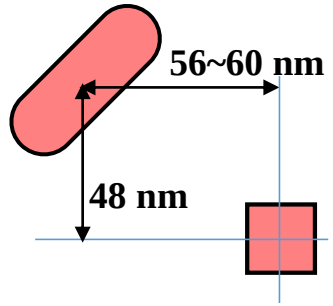
A SRAM Layout of 3 nm CFET



3 nm CFET SRAM Layout



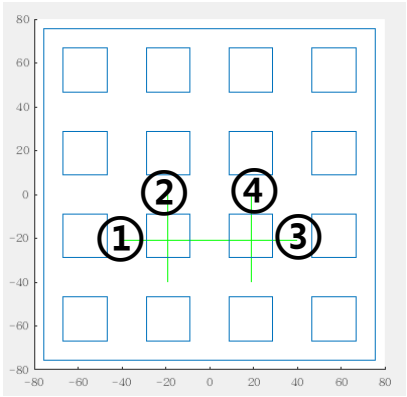
V0 can be realized by EUV LE3



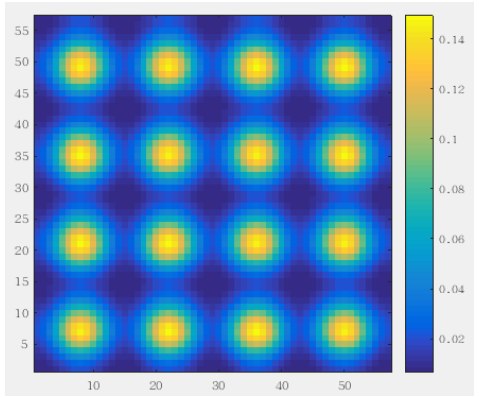
45° local interconnect design rule

- If 45º local interconnect is adopted, the SRAM area will be decreased from > 0.015 to ~0.011 μm^2.
- V0 can be divided into three masks, two of which involve 45º local connect design rules.
- The minimum area is ~2.6 squares for low NA EUV.
- We will study the process window of the 45º local interconnect design rule in high NA EUV lithography.

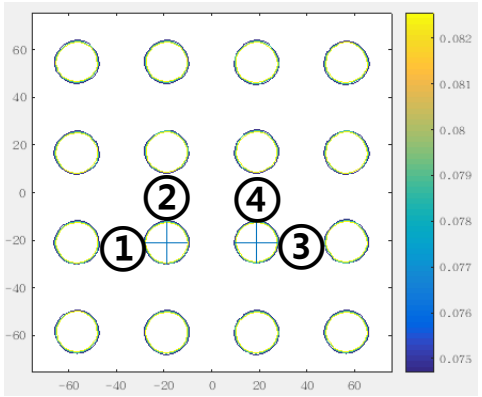
Anchor with pitch 28 nm design rule



Mask

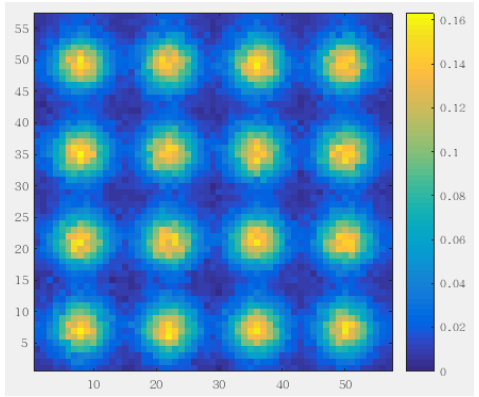


Aerial image

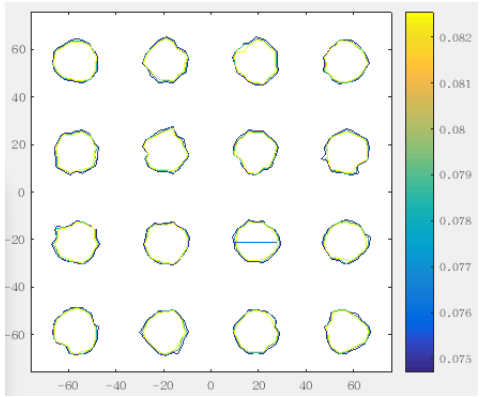


Contour

Line cut	①	②
EL	23.6%	24.2%
CD (nm)	18	17.5
Line cut	③	④
EL	24.6%	24.2%
CD (nm)	18	17.7



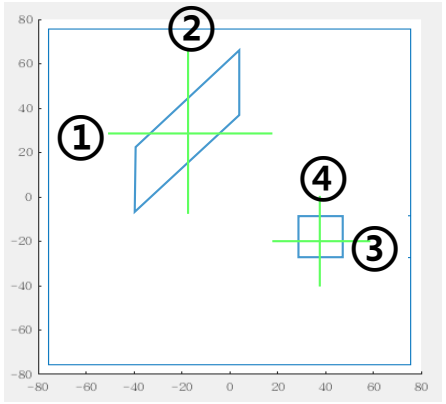
Aerial image with stochastics



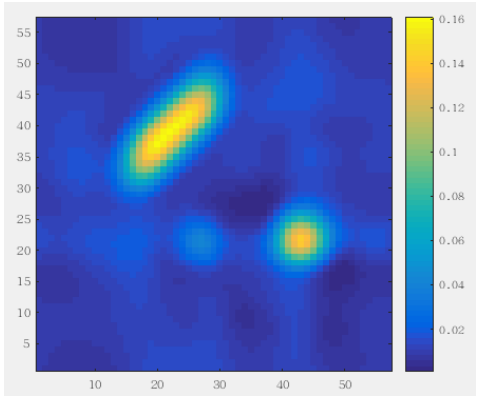
Contour with stochastics

- In 0.33 NA EUV lithography, the minimum line/space pitch is 36 nm and via pitch is 48~50 nm.
- In 0.55 NA EUV lithography, the minimum targeted line/space pitch is 28 nm and via pitch is ~38 nm.
- Via anchor pitch is 38 nm, ADI CD is 18 nm, EL ~ 24% > > 18% .
- Illumination: Annular 0.9/0.7; PR thickness: 30 nm.

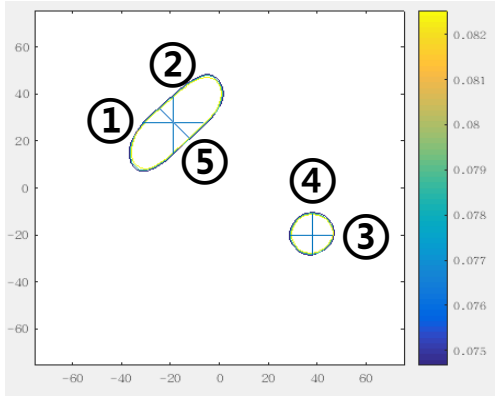
A 45° local interconnect exposed under High NA EUV



Mask

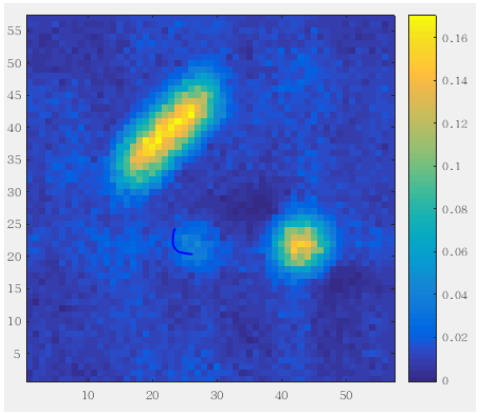


Aerial image

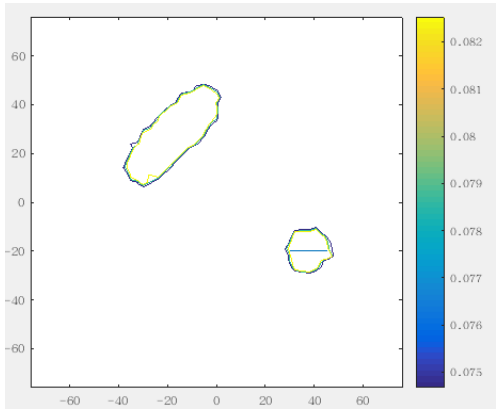


Contour

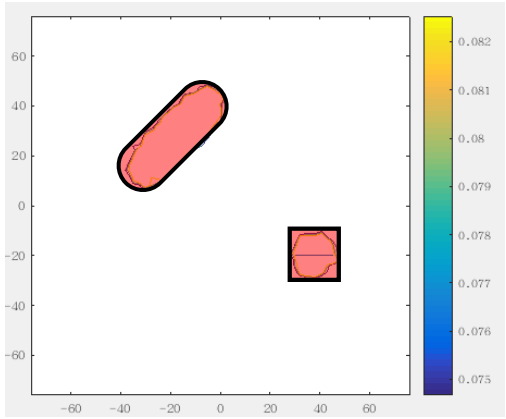
Line cut	①	②	③
EL	30.0%	29.0%	24.0%
CD (nm)	25.2	24.5	18
Line cut	④	⑤	
EL	23.0%	29.5%	
CD (nm)	17.6	17.6	



Aerial image with stochastics



Contour with stochastics



- The via CD is ~18 nm, EL is ~ 24% > > 18% .
- 45º local interconnect pattern CD is ~17.6 nm, EL is ~ 29% > > 18% , 3.6 squares for high NA EUV.
- This design rule can be easily implemented by high NA EUV lithography and the CFET SRAM area can be compressed.

Summary

- For 0.33 NA, the minimum pitch is 36 nm and the unbiased LWR is ~2.67 nm, which is comparable with the results from IMEC wafer data.
- For 0.55 NA, the minimum targeted pitch is 28 nm and the unbiased LWR can be improved to 2.2 nm.
- The TtT CD can be reduced from 20 nm of 0.33 NA EUV to 16 nm of high NA EUV lithography.
- Should we get a smaller TtT CD, such as 13 nm, we need to increase the exposure energy by ~15% in order to maintain the LWR to the original level of 2.2 nm.
- The minimum area of high NA EUV is about half that of 0.33 NA EUV lithography.
- The simulation results indicate that 90° bend and 45° local interconnect design rule are feasible in 0.55 NA EUV lithography. Both design rules can reduce masks of metal layer, and the latter design rule can compress the SRAM area.

THANKS